DIGITAL FILTER DESIGN FOR A PAL TV MODULATOR

Juha Yli-Kaakinen, Ming Hu, Teemu Kupiainen, and Markku Renfors

Department of Information Technology, Tampere University of Technology
P. O. Box 553, FIN-33101 Tampere, Finland, Email: mr@cs.tut.fi

ABSTRACT

This paper develops a baseband digital filter design for the Vestigial SideBand (VSB) filtering required in the traditional analog TV transmission system, PAL. In this application, a filter with relatively narrow passband and steep transition band is needed. Furthermore, the group delay specifications for the filter are demanding. An efficient solution satisfying the amplitude response specifications is developed based on Nth-band filters, which can be either of the FIR or the IIR type. The group delay response specifications can be satisfied by using either linear-phase FIR filters or approximately linear-phase IIR Nth-band filters. The latter approach seems to be more efficient for this application and it is developed further.

1. INTRODUCTION

THE traditional analog TV transmission systems have still a lifetime of many years, even though the new digital transmission techniques are being taken into use. In this situation, there is interest to more advanced implementation techniques for the traditional analog systems. For example, in CATV networks, the incoming TV signals are in many cases in digital format and also the modulators for new digital standards are using digital signal processing all the way to the IF stage. In this situation, it would be advantageous to be able to implement the analog TV modulation using digital signal processing techniques.

In this paper we consider the VSB filtering, which is an essential part of the modulator. Figure 1 shows the amplitude and group delay response specifications for the VSB filter for the PAL B/G system [1]. Here we consider implementing this filter assumed a complex baseband filter, which is quite feasible in case of digital signal processing, even though the analog VSB filtering is normally carried out at the IF stage.

The input signal is assumed to be a composite baseband video signal (i.e., it includes both the baseband luminance component and the chrominance components modulated to the color subcarrier) with 13.5 MHz sampling rate. Further, it is assumed that the input video signal is bandlimited from the low frequency end in such a way that there are no signal components which would disturb the audio carriers to be included in the complete video signal. Therefore, there is no need to implement the lower stopband part (below -5 MHz) of the specifications here. This means also that the audio components could be included in the signal already before the VSB filter. A suitable digital implementation of an audio modulator is described in [2].

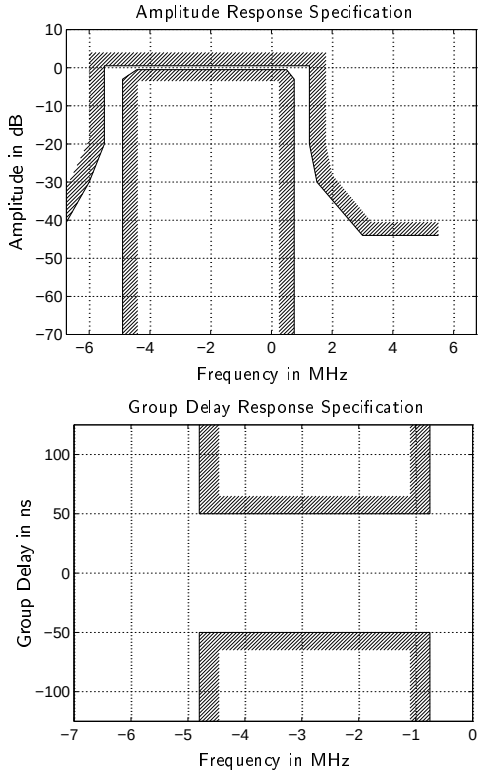

Fig. 1: Amplitude and group delay response specifications for the VSB filter for PAL system.

The outline of this paper is as follows. In Section 2 the efficient implementation of the VSB-filter is developed. The proposed desing is based on Nth-band filters. Both linear-phase FIR and approximately linear-phase IIR approaches have been considered. Section 3 involves finding the VSB-filter with simple coefficient representation forms. The target is to minimize the number of powers of two required for representing all the coefficients. In Section 4 ASIC implementation of the VSB-filter is described. Finally, the conclusions are given in Section 5

0–7803–5682–9/99/$10.00

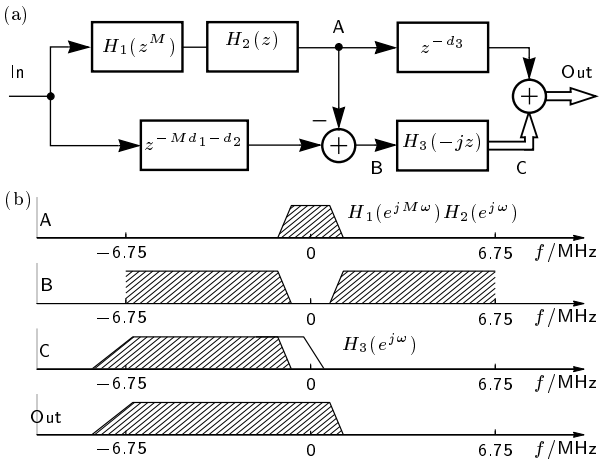

Fig. 2: The proposed VSB filter structure. (a) The overall structure. (b) Characteristic amplitude responses of the subfilters.

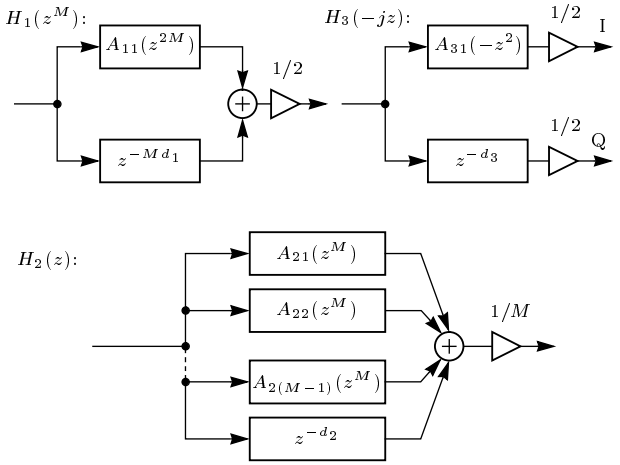

Fig. 3: Subfilter structures of the VSB filter based on approximately linear-phase recursive Nth-band filters.

2. FILTER DESIGN

One approach to design the filter would be to design a suitable lowpass filter and then translate it in the frequency axis in such a way that the required asymmetrical frequency response would be achieved. However, this would lead to a high filter order and complex signal processing in the implementation.

We have developed a multi-stage approach illustrated in Fig. 2. The idea is to divide the frequency band into two parts in such a way that the low-frequency band and the negative frequency axis part of the high-frequency band would constitute the VSB filtered signal. The positive and negative frequency parts of the high-frequency band are separated from each other using a phase-splitter $H_3(z)$ based on Hilbert-transformer [3]. In this approach, the transition band of the Hilbert-transformer is not very critical, and a low-order design is sufficient. Furthermore, the band-splitting filter can be implemented efficiently using Nth-band filters [4,5]. With the parameters of Fig. 1, both 6th-band and 8th-band filters would be feasible. By making preliminary designs for both cases, it was observed that the 8th-band case resulted in slightly lower implementation complexity. For the 8th-band filter, a cascade of halfband and 4th-band filters was considered to be the most efficient solution.

The Hilbert transformer is obtained by frequency-shifting a half-band prototype filter by $\pi/2$ [3]. Actually, the same design that is used for the half-band part of the band-splitting filter is used as the prototype for the Hilbert-transformer.

We have considered both linear-phase FIR [4] and IIR [5] type of Nth-band filters. In the IIR case, the Nth-band filters are based on parallel connection of allpass filters. In order to satisfy the strict group delay response specifications, the approximately linear-phase IIR Nth-band filters [5] are utilized. From these two alternatives, the IIR approach seemed to be more promising, as can be seen from Table 1, and it was chosen for further development. The different subfilters needed in the design are shown in Fig. 3. The required filter orders for the allpass sections of the IIR design are:

- $H_1(z)$, $H_3(z)$: branch 1 is a 4th-order allpass; branch 2 is a pure delay
- $H_2(z)$: branches 1, 2, and 3 are 2nd-order allpasses, branch 4 is a pure delay.

	FIR ($M=4$)	IIR ($M=3$)	IIR ($M=4$)
$H_1(z^M)$	4	6	4
$H_2(z)$	29	6	6
$H_3(jz)$	8	6	4
Total	41	18	16

Table 1: The required number of coefficients for the subfilters.

3. FILTER OPTIMIZATION

As the next step, the coefficients of the allpass sections in different filter stages were optimized using the algorithm developed in [6]. Allpass filter sections of the wave-digital lattice filter type were chosen [7].

In VLSI implementations, a significant reduction in hardware complexity is achieved, if the multiplication of a data sample by a constant adaptor coefficient is implemented using canonic-signed-digit (CSD) multiplier [8, 9]. The signed-digit representation of a fractional number has a general form

$$x = \sum_{r=1}^{R} a_r 2^{-P_r}, \qquad (1)$$

where each of the a_r's is either 1 or -1 and the P_r's are positive integers in increasing order. Therefore, the multiplication can be implemented as a sequence of shifts and adds. The CSD representation

:

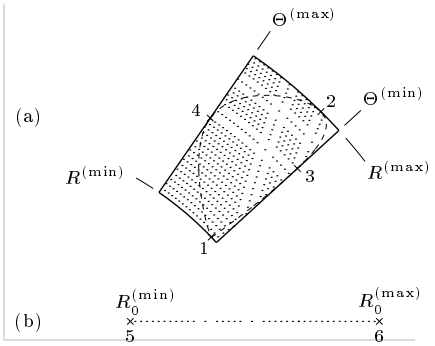

Fig. 4: Typical search spaces for the poles when three powers of two with 7 fractional bits ($R = 3$ and $P_R = 7$) are used for the adaptor coefficients. (a) Upper-half-plane pole for the complex-conjugate pole pair. (b) Real pole.

is a unique representation where the number of the additions, $R - 1$, is minimum.

It has turned out that a very straightforward quantization scheme for the filter coefficients is obtained as follows. For each complex-conjugate pole pair, the largest and smallest values for both the radius and angle are determined in such a way that by reoptimizing the locations of the remaining poles, the overall magnitude criteria can still be met. For each real pole, the smallest and largest values for the radius are found in a similar manner.

The above procedure gives for the upper-half-plane pole for each complex-conjugate pole pair the region $R\exp(j\Theta)$ where $R^{(\min)} \leq R \leq R^{(\max)}$ and $\Theta^{(\min)} \leq \Theta \leq \Theta^{(\max)}$, as illustrated in Fig. 4(a). The crosses numbered from 1 to 4 correspond, respectively, to the points where the smallest radius $R^{(\min)}$, the largest radius $R^{(\max)}$, the smallest angle $\Theta^{(\min)}$, and the largest angle $\Theta^{(\max)}$ are reached. Inside this region there is the feasible region given by dashed line in Fig. 4(a) where the pole can be located such that by relocating the remaining poles, the given overall criteria are still met by using infinite-precision arithmetic. For each real pole there is the corresponding region $R_0^{(\min)} \leq R \leq R_0^{(\max)}$ that is simultaneously the feasible region. In Fig. 4(b) the crosses numbered by 5 and 6 indicate $R_0^{(\min)}$ and $R_0^{(\max)}$, respectively.

The next step is to find in the above regions those pole locations which are achievable by implementing the adaptor coefficients using CSD coefficient representation. The dots in Fig. 4 indicate these pole locations. Note that the distributions are very irregular due to the desired representation form. All what is still needed is to check whether there exists a combination of the discrete pole positions with which the given overall criteria are met.

The optimization reduced the coefficient complexity significantly: considering CSD coefficient

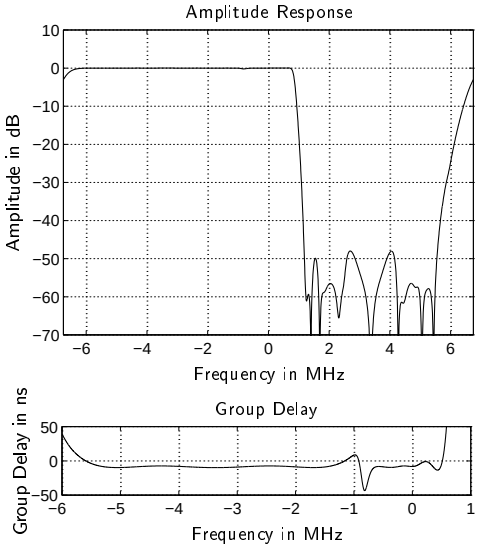

Fig. 5: Amplitude and group delay responses for the optimized design.

implementation, the number of adders/subtracters needed to implement all the adaptor coefficients for the overall design was reduced from 24 (obtained by direct rounding with minimum wordlength satisfying the specifications) to 9. For the optimized design, the maximum shift, P_R, required for the coefficient implementations is five for both $H_1(z)$ and $H_3(z)$. For $H_2(z)$, the corresponding figure is seven. On the other hand, for the FIR approach, the number of additions required for coefficient implementation, obtained by direct rounding, is 78 while the maximum shift is 14.

In addition to these adders needed for the coefficient implementation, the IIR structure includes 48 adders in the adaptors and for branch combining. The overall amplitude and phase responses of the design are shown in Fig. 5, and it can be seen that the specifications are satisfied quite well.

4. ASIC IMPLEMENTATION

As shown in Fig. 2 and Fig. 3, the VSB filter is constructed by using delay elements and first- and second-order allpass sections. Since the coefficients for the first- and second-order allpass sections are optimized as simple combinations of powers of two, a multiplication for each coefficient of the filter can be realized by a few simple shift operations and adders/subtracters.

The hardware description language VHDL was used to model hierarchically the designed VSB filter. Additional pipeline registers were inserted to the filter structure in Fig. 2 based on some estimations.

Parallel computational style was used for design simplicity. Positive edge-triggered static master-slave D flip-flops were used for delay elements for their robustness and ripple carry adders were used

for their small area and regularity.

The VHDL model simulation results were compared with MATLAB simulation results to verify the performance of the designed circuits and to determine the additional bits needed to satisfy finite wordlength effects. In order to avoid overflow and to satisfy round-off noise requirements, three more additional bits are needed when input is 13 bits sinusoidal test signal. Using 16 bit overall data wordlength (12 fractional bits, 3 integer bits and sign bit) in internal computations, the round-off noise level is well over 60 dB below the picture-carrier level of the PAL-modulated signal.

The VHDL model was synthesized for a 0.35 μm technology. The synthesis results are summarized in Table 2.

Data format	13-bit input and output 16-bit internal
Total area	2.6 mm^2
Layout density	14 000 gates/mm^2
Gate count	36 400
Operating clock frequency	13.5 MHz
Average power consumption	0.25 μW/MHz/gate
Power dissipation	123 mW at 13.5 MHz
Technology	0.35 μm, 3.3 V, 4-metal, n-well standard cell process

Table 2: Synthesis results.

5. CONCLUSION

We have developed for the VSB filter an efficient baseband digital filter design, which seems to be quite feasible for implementation as an application-specific integrated circuit.

In the continuation, we are going to study the possibilities to include a digital upconverter to convert the baseband video signal at the VSB filter output to the commonly used IF frequency of 38.9 MHz [10].

ACKNOWLEDGMENTS

This work was carried out in the project "Digital and Analog Techniques for Flexible Receivers" funded by the Technology Development Center of Finland (Tekes), Teleste Ltd, and other companies.

REFERENCES

[1] EN50083-5, "Cabled distribution systems for television and sound signals, part 5: Headend equipment," 1994, Cenelec.

[2] R. Uusikartano, J. Niittylahti, and M. Renfors, "Area-optimized FPGA implementation of a digital FM modulator," to appear in *IEEE Int. Conf. Circuits Syst.*, Orlando, FL, May 30–June 2 1999.

[3] P. A. Regalia, "Special filter design," in *Handbook for Digital Signal Processing*, S. K. Mitra and J. F. Kaiser, Eds., chapter 13, pp. 907–980. John Wiley and Sons, New York, 1993.

[4] F. Minzer, "On half-band, third-band, and Nth-band filters FIT filters and their design," vol. ASSP-30, pp. 734–738, Oct. 1982.

[5] M. Renfors and T. Saramäki, "Recursive Nth-band digital filters — Part I: Design and properties, Part II: Design of multistage decimators and interpolators," vol. CAS-34, no. 1, pp. 24–51, Jan. 1987.

[6] J. Yli-Kaakinen and T. Saramäki, "An efficient algorithm for the design of lattice wave digital filters with short coefficient wordlength," to appear in *Proc. IEEE Int. Symp. Circuits Syst.*, May 30–June 2 1999.

[7] M. Renfors and E. Zigouris, "Signal processor implementation of digital all-pass filters," vol. ASSP-36, no. 5, pp. 714–729, May 1988.

[8] A. Avizenis, "Signed digit number representation for fast parallel arithmetic," *IRE Trans. in Electronic Computers*, vol. EC-10, pp. 383–400, Sept. 1961.

[9] R. I. Hartley, "Subexpression sharing in filters using canonic signed digit multipliers," vol. 43, no. 10, pp. 677–688, Oct. 1996.

[10] J. Yli-Kaakinen, T. Kupiainen, Ming Hu, R. Uusikartano, and M. Renfors, "Digital filter design for a PAL TV modulator," to appear in *Proc. IEEE Int. Conf. Consumer Electronics* (ICCE'99), Los Angeles, CA, June 22–24 1999.