Multirate Charge-Domain Filter Design for RF-Sampling Multi-Standard Receiver

Juha Yli-Kaakinen, Vesa Lehtinen, and Markku Renfors

***Abstract*—This paper proposes a reconfigurable decimator architecture for a multi-standard receiver front-end. This architecture is based on direct radio-frequency bandpass sampling and analog discrete-time multirate signal processing. The overall front-end consists of a low-noise amplifier followed by a tunable charge-domain sampler, a reconfigurable decimator, and an analog-to-digital converter. The proposed decimator is constructed as a cascade of four switched-capacitor filtering stages. The frequency responses and the decimation factors of these stages are digitally controllable thus enabling high reconfigurability. The advantages of the proposed design are a high image rejection, a low overall implementation complexity, and high flexibility. The feasibility of the design is evaluated by computer simulations.**

***Index Terms*—RF sampling, direct sampling, software-defined radio, multi-standard receiver, switched-capacitor filters.**

I. Introduction

ANALOG receiver front-end processing is facing new challenges and provides also new opportunities. In low-cost implementations, deep sub-micron, i.e., nano-scale very large-scale integration (VLSI) processing optimized for digital circuits are to be used also for analog radio frequency (RF) circuitry. Reduced supply voltage leads to reduced linear range of amplifiers, and there are difficulties in implementing receivers based on the conventional superheterodyne or direct-conversion principles. Digital complementary metal oxide semiconductor (CMOS) processes have very limited voltage headroom that leads to the situation where the time-resolution of a digital signal edge transition is superior to voltage resolution of analog signals. Charge-domain sampling and analog discrete-time processing are found to be suitable basic techniques with such processes [1], [2].

Moving towards multi-standard radio, a high level of integration becomes necessity and can only be accomplished by new improved radio architectures. Major improvements are required also for the analog RF front-end which should handle a large range of carrier frequencies, possess a flexible bandwidth, and cope with a severe dynamic range requirements and wide variety of operational conditions. A possible solution is to transfer the signal sampling and analog-to-digital interface from baseband to higher frequencies. However, the relatively slow development of analog-to-digital converter (ADC) technologies, in comparison to the extremely fast progress of digital VLSI circuits, is the main bottleneck when developing DSP-based solutions for the receiver front-end functionalities. This calls for innovative solutions regarding the partitioning of the functionalities to the analog and digital domains.

Analog discrete-time switched-capacitor filters based on deep-submicron CMOS technology have recently become popular in RF radio front-end designs due to their excellent RF performance, low power consumption, and a high level of integration [2]–[5]. The fact that the switched-capacitor filters can be made digitally reconfigurable makes RF sampling very appealing in terms of building multi-standard radio [1], [6]. Furthermore, since the transistors are used as switches their nonlinearities become less important and less susceptible to process scaling.

Receiver structures based on sampling directly at RF frequencies are better suited to the VLSI technology trends. These novel, so-called digital radio processor architectures perform automatic gain control, down-conversion, and channel filtering using discrete-time analog signal processing [2], [4], [7]. Most of the receiver selectivity can then be done in a flexible way, at or close to baseband, before the ADC. This relieves the requirements for high-speed, high-resolution ADCs, which tend to lead to very high power consumption. It is clear that there are great challenges in making such designs feasible for the more wideband wireless standards. This contribution focuses on the optimization of key modules (sampler with embedded filtering and decimating analog discrete-time filters) for such receiver RF front-ends. The simulations shown that the performance of the proposed approach compares favorably with other switched-capacitor based approaches proposed in the litterature.

The paper is organized as follows. In Section II, the proposed decimator architecture for a multi-standard RF front-end is introduced and the target specifications are briefly reviewed. In Section III, the multistage implementations of the sampling rate converters are revised and the requirements for the substages are defined. In addition, this section shortly introduces the filter structures suitable for implementing the substages. The discrete-time transfer functions of the decimator are given in Section IV whereas the corresponding reconfigurable charge-domain models, which are the main contribution of this paper, are described in detail in Section V. In Section VI, the frequency responses of the proposed design are verified through simulations and sensitivity analysis is carried out to ensure the feasibility of the decimator design. Finally, the conclusions are drawn in Section VII.

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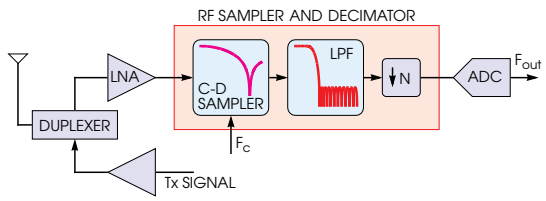

Fig. 1. General block diagram of the receiver front-end.

II. Architecture for Multi-Standard Receiver

The block diagram of the general receiver front-end under consideration in this contribution is shown in Fig. 1. This front-end consists of a duplexer and a low-noise amplifier (LNA) followed by a charge-domain sampler [1], a reconfigurable analog discrete-time decimator [8], and a $\Sigma\Delta$ analog-to-digital converter (ADC). For simplicity, only the in-phase branch of the front-end is shown in Fig. 1 and a similar structure has to be duplicated for the quadrature branch.

In the sampler block, the incoming amplified RF signal is first sampled at the carrier frequency F_c through the charge-domain sampler. This sampling inherently down-converts the signal to the baseband such that the sample rate of the resulting continous-valued output signal is equal to the carrier frequency. The down-converted signal is then decimated by means of a passive switched-capacitor filter prior to analog-to-digital conversion. The specifications for the decimator are selected such that the frequency response of the overall filter approximately satisfies the system-specific channel selectivity requirements while each stage has been designed to suppress at a tolerable level those signal components that will alias into the passband. Finally, the down-sampled and down-converted analog discrete-time signal is converted into the digital domain using ADC.

In this implementation, the frequency-domain characteristics are determined by the sampler sampling rate F_c as well as by the clock and control signals of the decimator. The receiver front-end can be tuned to a different frequency band by simply changing the sampling rate whereas the channel bandwidth and the selectivity can be controlled by clock signals. This makes the receiver architecture fully reconfigurable and well suited for multi-standard applications.

The quadrature component can be captured using another identical branch that also samples at rate F_c but at a time shift that corresponds to quarter cycle of the RF center frequency [9]. For narrowband signals, this so-called second-order sampling approach provides a close approximation of the ideal complex quadrature sampling. With increasing channel bandwidth, there will be phase mismatch and the resulting error can be modeled as I/Q imbalance that increases with increasing distance from the center frequency [10]. This effect is characterized by the minimum attenuation of the image bands at the channel edge frequencies. These I/Q-imbalance effects are practically insignificant in cases to be considered in this paper. For higher channel bandwidths, this effect can be straightforwardly compensated in the baseband [10].

Two divergent cases are considered as example communication systems in order to validate the reconfigurability of the proposed implementation. For the first case, the bandwidth of the signal is relatively wide making it suitable for wideband wireless standards such as 802.11a/g/n, whereas the second case considers narrowband standards such as GSM/EDGE and Bluetooth. In the sequel, designs satisfying wideband and narrowband requirements are denoted as *Case A* and *Case B* designs, respectively. It should be pointed out that the proposed architecture can be generalized also for other wireless standards.

The specifications for the overall decimation and channel selection filter are stated as

$$1-\delta_p \le |H(e^{j2\pi f/F_s})| \le 1+\delta_p \quad \text{for } f \in [0, f_p] \tag{1a}$$

$$|H(e^{j2\pi f/F_s})| \le \delta_s \quad \text{for } f \in X_s. \tag{1b}$$

In these specifications, f_p, the passband edge frequency of the overall filter, corresponds to half the channel bandwidth of interest of the communication standard under consideration, whereas the stopband region

$$X_s = \bigcup_{n=1}^{\lfloor N/2 \rfloor} \left[\frac{(2n-\rho)F_s}{2N}, \min\left\{ \frac{(2n+\rho)F_s}{2N}, \frac{F_s}{2} \right\} \right] \tag{2}$$

with $\rho = Nf_p/(F_s/2)$ is determined to prevent aliasing into the passband region. As a consequence of the suppression of the aliasing terms, the power of the out-off-band blockers is reduced as well. In the proposed front-end, most of the channel selection filtering is carried out in the analog domain, however, in order to meet the strict blocking requirement of the GSM standard the final channel filtering should be performed in the digital domain.

For two cases under consideration, it is desired that the decimation filter satisfies the specifications of (1) as follows. For *Case A* design, $f_p = 12.5$ MHz and the maximum allowable passband and stopband ripples are $\delta_p = 0.0288$ ($A_p = 0.5$ dB) and $\delta_s = 5.6234 \cdot 10^{-4}$ ($A_s = 65$ dB), respectively, whereas for *Case B* design, $f_p = 100$ kHz, $\delta_p = 0.01151$ ($A_p = 0.2$ dB), and $\delta_s = 10^{-5}$ ($A_s = 100$ dB) [11], [12].

III. Decimation Filter Implementation

In order to alleviate the requirements for the decimating filters, it is beneficial to carry out the decimation in several stages [13]. For the proposed design, the overall filter roughly satisfies the system-specific channel selectivity requirements while the substages have been designed to suppress the aliasing signal components.

If the sample rate conversion ratio can be factored into the product

$$N = N_1 N_2 \cdots N_L, \tag{3}$$

where $N_1, N_2, \ldots, N_L$ are integers, then the overall decimation by the factor of N can be implemented using L stages [13]. In order to clarify the analysis and determination of the roles of the sub-blocks in providing the desired decimation by the overall factor of N, it is advantageous to represent the multi-stage implementation by its equivalent single-stage model. In this equivalent, only one filter with transfer function

$$H(z) = H_1(z)H_2(z^{N_2}) \cdots H_L(z^{N_2 N_3 \cdots N_L}) \tag{4}$$

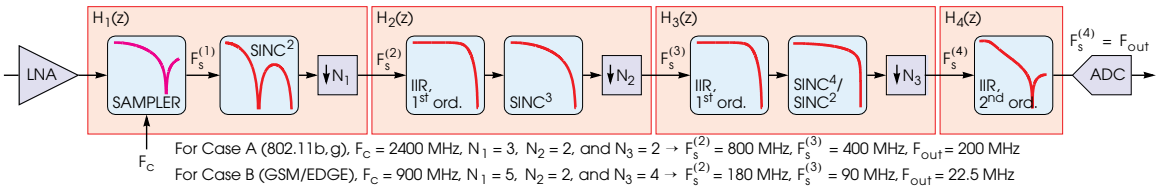

Fig. 2. Block diagram of a receiver front-end showing all the substages.

is involved followed by down-sampling by a factor of N.

The proposed approach incorporates cascades of IIR and FIR filters as the substages of the proposed multistage decimator. The extremely simple filter structures suitable for passive charge-domain signal processing are so-called all-pole IIR filters and running-sum FIR filters [2], [3], [6], [14].

In order to increase the flexibility and to minimize the implementation cost by reusing the common blocks in both designs, the transfer functions $H_\ell(z)$ for $\ell = 1, 2, \ldots, L$ are implemented as a cascades of IIR and FIR filters as follows:

$$H_\ell(z) = G_\ell(z)F_\ell(z), \tag{5a}$$

where

$$G_\ell(z) = \prod_{n=1}^{P_\ell} G_\ell^{(n)}(z) \quad \text{and} \quad F_\ell(z) = \prod_{n=1}^{Q_\ell} F_\ell^{(n)}(z). \tag{5b}$$

Here, $G_\ell^{(n)}(z)$'s are either the transfer functions of periodic all-pole filters as expressed by

$$G_\ell^{(n)}(z) = a_\ell^{(n)}/(1 + b_\ell^{(n)} z^{-S_\ell^{(n)}}) \tag{6a}$$

with $a_\ell^{(n)} = b_\ell^{(n)}+1$ or the transfer functions of the second-order all-pole filters as given by

$$G_\ell^{(n)}(z) = a_\ell^{(n)}/(1 + b_\ell^{(n)} z^{-1} + c_\ell^{(n)} z^{-2}). \tag{6b}$$

The transfer functions $F_\ell^{(n)}(z)$, in turn, are cascaded linear-phase running-sum FIR filters as expressed by

$$F_\ell^{(n)}(z) = R_\ell(z)^{K_\ell^{(n)}}, \tag{7a}$$

where the transfer functions of the running-sum filters are as follows:

$$R_\ell(z) = \sum_{m=0}^{M_\ell^{(n)}-1} z^{-m}. \tag{7b}$$

Here, $M_\ell^{(n)}$ is the order of the running-sum FIR filter and $K_\ell^{(n)}$ corresponds to the number of cascaded identical running-sum filter blocks. When these filters are used for decimation, $M_\ell^{(n)}$ corresponds to the decimation factor.

IV. Discrete-Time Models for the Subfilters

The block diagram of the in-phase branch for the proposed overall system is depicted in Fig. 2. In this implementation, the overall anti-imaging and channel selection filtering is divided into four stages ($L = 4$). This selection reduces the requirements of the subfilters and increases the configurability to meet the specifications of multiple wireless standards.

In order to utilize efficiently the oversampling in the ΣΔ A/D conversion and to obviate the need of power consuming high-speed A/D converter the sample rates at the output of the decimator are chosen to be 200 MHz and 22.5 MHz for *Case A* and *Case B* designs, respectively. These output sampling rates can be achieved, e.g., by choosing $N_1 = 3$, $N_2 = 2$, $N_3 = 2$, and $N_4 = 1$ for *Case A* design and $N_1 = 5$, $N_2 = 2$, $N_3 = 4$, and $N_4 = 1$ for *Case B* design. In this case, the overall sample rate reduction factor is $N = 12$ and $N = 40$ for *Case A* and *Case B* designs, respectively.

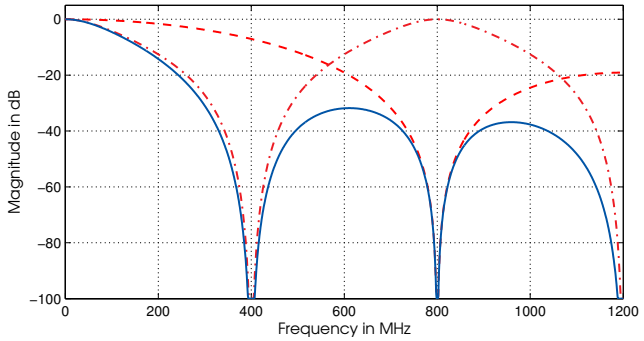

Fig. 3. Magnitude responses at the first and second decimation stages for *Case A* design. The solid line shows the response for $H_1(z)H_2(z^3)$ whereas the dashed and dot-dashed lines show the responses for $H_1(z)$ and $H_2(z^3)$, respectively.

A. First Decimation Stage

For achieving efficient charge-domain implementations, the first decimation stage consist of single FIR filter, as given by (7), as the only building block [$P_\ell = 0$ and $Q_\ell = 1$ in (5b)]. For $K_1^{(1)} = 1$, the theoretical minimum attenuation of the aliasing components is only 34.4 dB and 64.6 dB for *Case A* and *Case B* designs, respectively. Therefore, $K_1^{(1)}$ should be increased. The given specifications are met for both cases under consideration by choosing $K_1^{(1)} = 2$, that is, $H_1(z)$ is given by

$$H_1(z) = F_1^{(1)}(z) = \begin{cases} (1 + z^{-1} + z^{-2})^2 & \text{for } \textit{Case A} \\ (\sum_{m=0}^{4} z^{-m})^2 & \text{for } \textit{Case B}. \end{cases} \tag{8}$$

In this case, the resulting theoretical minimum attenuation of the aliasing components is 72.7 dB and 129.3 dB for *Case A* and *Case B* designs, respectively. The magnitude response of $H_1(z)$ for *Case A* design is shown in Fig. 3.

B. Second Decimation Stage

The transition bandwidths of the second decimation stage are reduced compared with those of the first stage. Therefore, increased selectivity is required for the anti-aliasing filters and, consequently, this stage consist of both the single IIR filter and

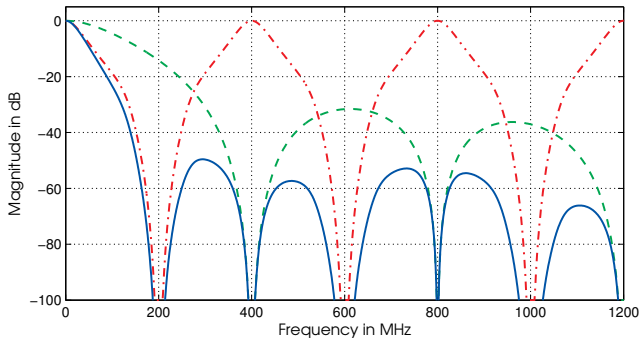

Fig. 4. Magnitude responses at the third decimation stage for *Case A* design. The solid line shows the response for $H_1(z)H_2(z^3)H_3(z^6)$ whereas the dashed and dot-dashed lines show the responses for $H_1(z)H_2(z^3)$ and $H_3(z^6)$, respectively.

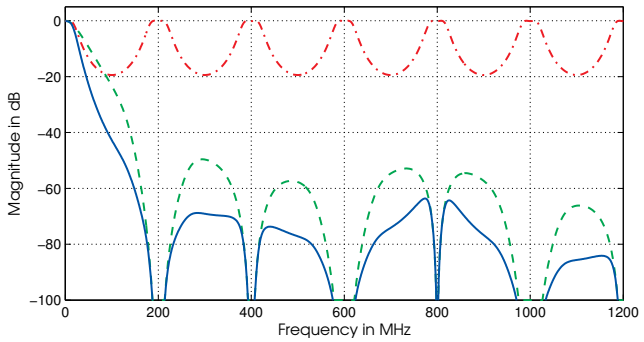

Fig. 5. Magnitude responses at the fourth stage for *Case A* design. The solid line shows the response for $H_1(z)H_2(z^3)H_3(z^6)H_4(z^{12})$ whereas the dashed and dot-dashed lines show the responses for $H_1(z)H_2(z^3)H_3(z^6)$ and $H_4(z^{12})$, respectively.

the single FIR filter, that is, the transfer function is expressed as

$$H_2(z) = G_2^{(1)}(z)F_2^{(1)}(z). \tag{9a}$$

Here, $G_2^{(1)}(z)$ is a periodic all-pole filter as given by (6a) with $S_2^{(1)} = 2$ and $b_2^{(1)} = -0.2$ or $b_2^{(1)} = -0.8$ for *Case A* and *Case B* designs, respectively. For simplicity of the presentation, $F_2^{(1)}(z)$ is chosen to be equal for both designs and the desired attenuation is achieved by selecting $K_2^{(1)} = 3$, that is, the transfer function of the FIR part is given by

$$F_2^{(1)}(z) = (1 + z^{-1})^3 = 1 + 3z^{-1} + 3z^{-2} + z^3. \tag{9b}$$

The IIR part can be implemented with the very small additional circuitry as will be seen in Subsection V-B. The theoretical stopband attenuation for the resulting filter is 91.2 dB and 174.0 dB for *Case A* and *Case B* designs, respectively. The magnitude responses for the substages are depicted in Fig. 3 for *Case A* design.

C. Third Decimation Stage

Third stage reduces the sampling rate at the final output sample rate. The selectivity requirements for this stage are further increased and consequently the complexity of the filters is increased as well. The specifications are met by realizing $H_3(z)$ as follows

$$H_3(z) = F_3(z)\prod_{n=1}^{3} G_3^{(n)}(z). \tag{10}$$

Here, $G_3^{(n)}(z)$'s are the transfer functions of the all-pole filters, as given by (6a), with $b_3^{(1)} = -0.2$, $b_3^{(2)} = -0.14286$, and $b_3^{(3)} = -0.2$ for *Case A* design and with $b_3^{(1)} = -0.6$, $b_3^{(2)} = -0.61539$, and $b_3^{(3)} = -0.57143$ for *Case B* design. The periodicities of the transfer functions are $S_3^{(n)} = n$ for $n = 1, 2, 3$ [cf. (6a)]. The transfer function of the FIR part, in turn, is given by

$$F_3(z) = \begin{cases} (1 + z^{-1})^4 & \text{for } \textit{Case A} \\ (1 + z^{-1} + z^{-2} + z^{-3})^2 & \text{for } \textit{Case B}. \end{cases} \tag{11}$$

The FIR part can be further factorized into three substages in order to minimize the implementation complexity. This factorization is given by

$$F_3(z) = F_3^{(1)}(z)F_3^{(2)}(z)F_3^{(3)}(z), \tag{12a}$$

where for *Case A* design

$$F_3^{(n)}(z) = \begin{cases} 1 + z^{-1} & \text{for } n = 1 \quad (12b) \\ 1 + z^{-1} & \text{for } n = 2 \quad (12c) \\ 1 + 2z^{-1} + z^{-2} & \text{for } n = 3, \quad (12d) \end{cases}$$

whereas for *Case B* design

$$F_3^{(n)}(z) = \begin{cases} 1 + z^{-1} & \text{for } n = 1 \quad (12e) \\ 1 + z^{-2} & \text{for } n = 2 \quad (12f) \\ 1 + z^{-1} + z^{-2} + z^{-3} & \text{for } n = 3. \quad (12g) \end{cases}$$

In this case, the sum of the coefficients in (12b) and (12e), (12c) and (12f), as well as in (12d) and (12g) are equal and, therefore, these terms can share most of their circuitry as will be shown in Section V-C.

The resulting minimum attenuation of the aliasing components in the case of *Case A* design is 108.4 dB whereas for the *Case B* design the corresponding value is 141.4 dB. Figure 4 shows the magnitude responses of the subfilters for *Case A* design.

D. Last Filtering Stage

The purpose of the last stage is to carry out the final channel shaping while the earlier filtering stages act mainly as the anti-alias filters. The last stage consist only of an IIR filter, that is $H_3(z) = G_4^{(1)}(z)$ where $G_4^{(1)}(z)$ is a second-order all-pole filter as given by (6b) with $a_4^{(1)} = 0.54155$, $b_4^{(1)} = -1.59363$, and $c_4^{(1)} = 0.67459$ for *Case A* design and $a_4^{(1)} = 0.99285$, $b_4^{(1)} = -1.93237$, and $c_4^{(1)} = 0.93435$ for *Case B* design. Here, the coefficient values are optimized according to the specifications of the target wireless communication standard. This optimization has been performed in such a manner that the maximum allowable component values (capacitances) of the final realization are constrained to be smaller than certain prescribed value. Figure 5 shows the magnitude responses for the overall implementation as well as that of the subfilters for *Case A* design.

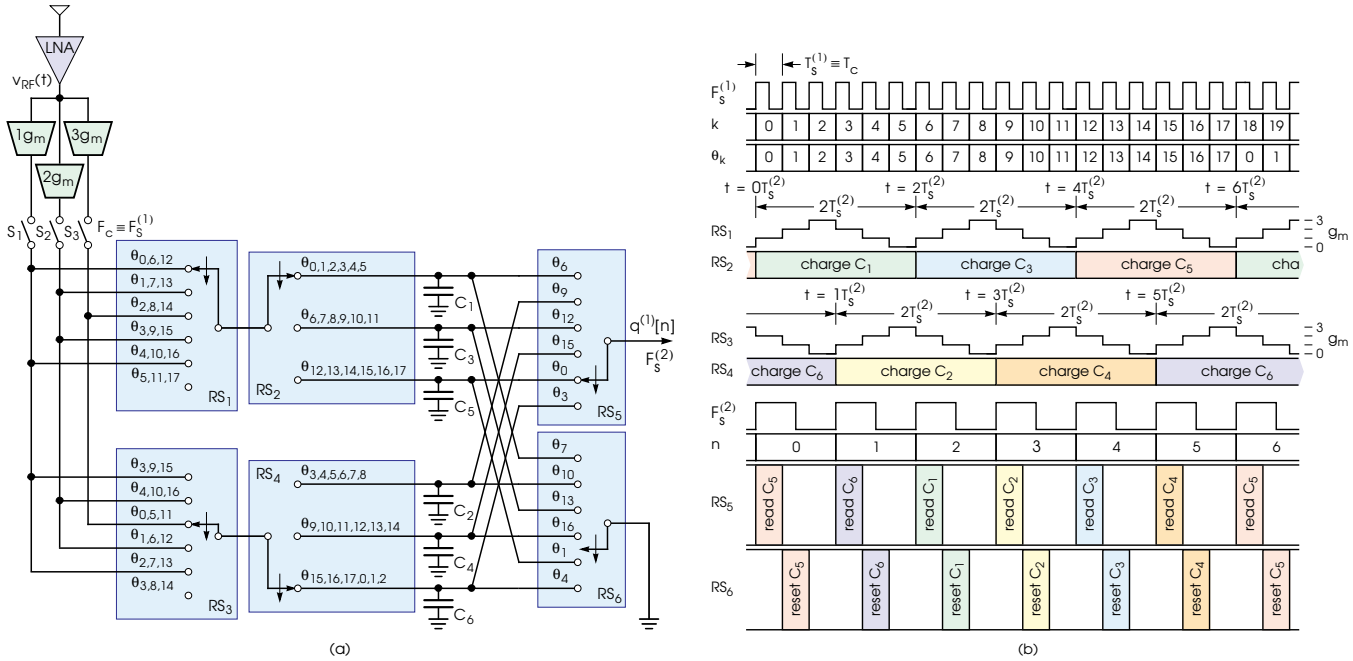

Fig. 6. (a) Charge-domain commutator-switch model of the first decimation stage $H_1(z)$ for *Case A* design. (b) The corresponding timing diagram.

V. Charge-Domain Models of the Subfilters

This section describes in detail the charge-domain models of the discrete-time filters derived in Section IV. In these models, the first stage is based on the weighted integrative sampling of the current signals. This concept is proposed for conventional FIR filters in [15]. In this contribution this technique is extended for realizing highly selective decimators with possibly configurable sampling rate conversion factor. The second stage is based on time-interleaved charge sharing between weighted capacitor values. The time-interleaved implementation of decimating switched-capacitor filters based on charge sharing is first studied in [16]. In the proposed implementation, this scheme is combined with the weighted integrative sampling such that the composed filter realizes the cascade of two decimation stages in a very effective manner. In the third stage, the decimator is realized as a cascade of very simple basic building blocks resulting in highly flexible overall filter. The fourth stage is based on a second-order filter described in [14]. For the slightly modified filter, an optimization algorithm was designed to determine optimal capacitor values.

A. First Decimation Stage

The commutator-switch model of the charge-domain sampler with embedded first FIR decimation filter $F_1^{(1)}(z)$ is illustrated in Fig. 6(a) for *Case A* design. In this implementation, three transconductors with gains g_m, $2g_\mathrm{m}$, and $3g_\mathrm{m}$ convert the received RF voltage $v_\mathrm{RF}(t)$ into the corresponding currents $i_\mathrm{RF}(t) = g_\mathrm{m} v_\mathrm{RF}(t)$, $2i_\mathrm{RF}(t) = 2g_\mathrm{m} v_\mathrm{RF}(t)$, and $3i_\mathrm{RF}(t) = 3g_\mathrm{m} v_\mathrm{RF}(t)$. When $F_s^{(1)} \equiv F_c$ is high, switches S_r for $r = 1, 2, 3$ are closed and the currents delivered by the transconductors are integrated cyclically into six identical sampling capacitors C_r for $r = 1, 2, \ldots, 6$ through four rotating switches RS_r for $r = 1, 2, 3, 4$.

The current is first integrated into C_1 through rotating switch RS_2 for six clock cycles of $F_s^{(1)}$, denoted by θ_k for $k = 0, 1, \ldots, 5$ in Figs. 6(a) and 6(b), such that the current, as selected by RS_1, is $i_\mathrm{RF}(t)$ on θ_0 and θ_4; $2i_\mathrm{RF}(t)$ on θ_1 and θ_3; $3i_\mathrm{RF}(t)$ on θ_2; and zero on θ_5. For the following six clock cycles, denoted by θ_k for $k = 6, 7, \ldots, 11$, the current is integrated in the same manner into C_3 and on θ_k for $k = 12, 13, \ldots, 17$ into C_5.

Similarly, rotary switch RS_4 charges capacitors C_2, C_4, and C_6 such that on θ_k for $k = 3, 4, \ldots, 8$ the current is integrated into C_2 whereas on θ_k for $k = 9, 10, \ldots, 14$ into C_4 and on θ_k for $k = 15, 16, 17, 0, 1, 2$ into C_6. This integration scheme is carried on sequentially for the forthcoming samples as illustrated in Fig. 6(b).

In this time-interleaved cyclical integration arrangement, the gains of the transconductors correspond to the impulse response values of the first anti-aliasing filter $F_1^{(1)}(z)$ as given for *Case A* design by

$$F_1^{(1)}(z) = 1 + 2z^{-1} + 3z^{-2} + 2z^{-3} + z^{-4}. \tag{13}$$

After each current integration period, the charges from the C_r's are transferred to a subsequent stage through commutator RS_5 at the rate of $F_s^{(2)} = F_s^{(1)}/3 \equiv F_c/3$ and the sampling capacitors are discharged through commutator RS_6 prior to integration of new samples.

In this model, time-interleaving is used to maintain the desired output sample rate. For single sampling capacitor, the number of clock cycles needed to produce one output sample is seven, that is, five clock cycles are used for charging the capacitor, one cycle for charge readout, and one for discharging. However, the decimation factor is three, that is, the output has to be generated on every third clock cycle and, consequently, several time-interleaved capacitors have to be used for reaching the desired output rate. In this case, the minimum number of capacitors required is only three compared

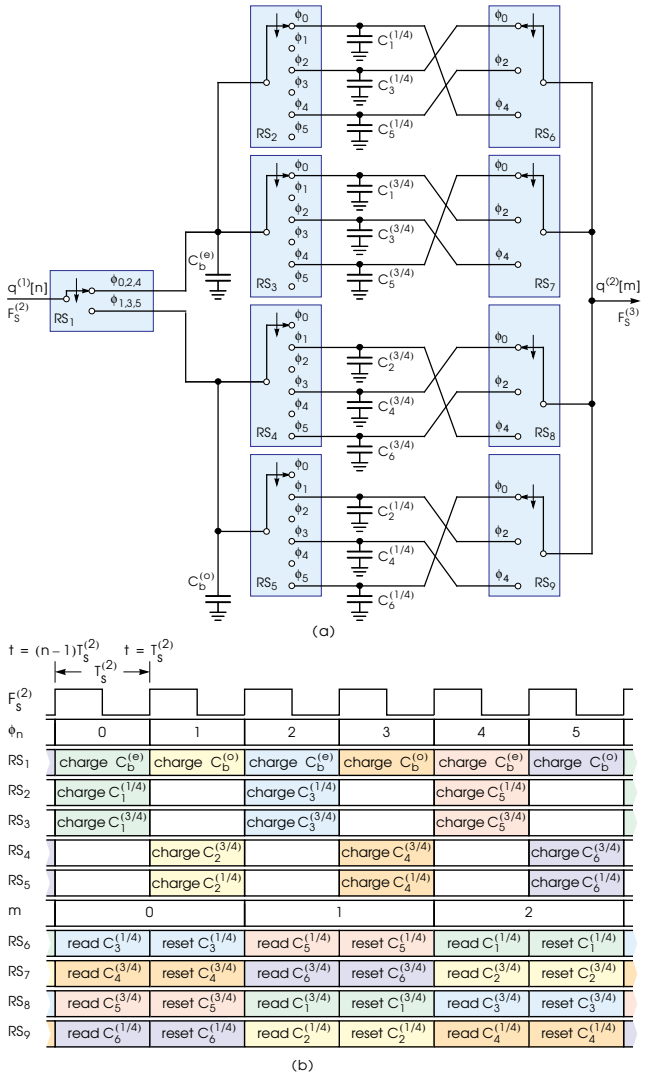

Fig. 7. (a) Charge-domain commutator-switch model of the second decimation stage for both the *Case A* and *Case B* designs. (b) A timing diagram.

with six capacitors used in the model of Fig. 6. However, as will be seen later on in this contribution these three additional capacitors simplify the overall implementation by allowing the capacitors to be shared between two consecutive stages.

Let $q_1[n]$ be the total amount of charge integrated into the capacitors on charging period of five clock cycles. Neglecting circuit non-idealities and assuming that the integrator performs perfect integration of the current samples the charge integrated into C_r at the nth sampling instant can be written as

$$q_1[n] = q_1(nT_s^{(2)}) = \sum_{k=0}^{4} f_1[k] g_\mathrm{m} \int_{nT_s^{(2)}-kT_s^{(1)}-T_i}^{nT_s^{(2)}-kT_s^{(1)}} v_\mathrm{RF}(t)\mathrm{d}t, \tag{14}$$

where $T_s^{(1)} = 1/F_s^{(1)} \equiv 1/F_c$ is the time delay between two input current samples, $T_s^{(2)} = 1/F_s^{(2)}$ is the output sampling period, $T_i = T_s^{(1)}/2$ is the integration period, and $f_1[k]$ for $k = 0, 1, \ldots, 4$ are the impulse response values of $F_1(z)$.

The frequency response of this structure can be determined by evaluating the integral in (14) yielding

$$H_1(\mathrm{j}2\pi f) = H_c(\mathrm{j}2\pi f) F_1^{(1)}(\mathrm{e}^{\mathrm{j}2\pi f T_s^{(1)}}), \tag{15}$$

where $H_c(\mathrm{j}2\pi f)$ is the response due to the integration of the current within a rectangular time window whereas $F_1^{(1)}(\mathrm{e}^{\mathrm{j}2\pi f T_s^{(1)}})$ is the frequency response of the first discrete-time FIR anti-aliasing filter resulting from the summation of the five weighted time-delayed current samples.

For *Case B* design, the integration is carried out over nine current samples instead of the five samples of *Case A* design and the charge from the sampling capacitors is transferred at the rate of $F_s^{(1)} = F_s^{(2)}/5 \equiv F_c/5$. The corresponding model requires two additional transconductors with gains of $4g_\mathrm{m}$ and $5g_\mathrm{m}$. This structure can be straightforwardly generalized also to other decimation factors and parameters $K_\ell^{(n)}$ [cf. (7)].

B. Second Decimation Stage

The commutator-switch model of the second decimation stage for both *Case A* and *Case B* designs is shown in Fig. 7(a). In this model, the charge integrated in the previous stage is cyclically transferred to parallel capacitors such that for even (odd) samples the charge is transferred to feedback capacitor $C_\mathrm{b}^{(\mathrm{e})}$ ($C_\mathrm{b}^{(\mathrm{o})}$) and one of the feedforward capacitors $C_r = C_r^{(1/4)} + C_r^{(3/4)}$ for $r = 1, 3, 5$ ($r = 2, 4, 6$). The feedforward capacitors C_r for $r = 1, 2, \ldots, 6$ are chosen such that $C_1 = C_2 = \cdots = C_6$ and $C_r^{(3/4)} = 3C_r^{(1/4)}$ for $r = 1, 2, \ldots, 6$ whereas for feedback capacitors $C_\mathrm{b}^{(\mathrm{e})} = C_\mathrm{b}^{(\mathrm{o})}$.

At the beginning of each sampling period the C_r's are empty due to a reset phase. The feedback capacitors $C_\mathrm{b}^{(\mathrm{e})}$ and $C_\mathrm{b}^{(\mathrm{o})}$ are never discharged, and thus they hold some charge corresponding to the voltages from the previous sampling periods. The discharging circuitry is not illustrated in Fig. 7(a) and in the following figures due to its simplicity. However, the resetting cycles are still shown in Fig. 7(b) and in the following timing diagrams.

In this model, the even and odd input samples are processed separately. On the first even clock cycle of $F_s^{(2)}$ denoted by ϕ_0 in Figs. 7(a) and 7(b), the charge is transferred into parallel $C_\mathrm{b}^{(\mathrm{e})}$ and $C_1 = C_1^{(1/4)} + C_1^{(3/4)}$ through rotating switches RS_r for $r = 1, 2, 3$. The total charge stored on $C_\mathrm{b}^{(\mathrm{e})}$ and $C_r = C_1$ after this first even sampling instant is expressed as

$$q_\mathrm{t}[n] = q_\mathrm{b}[n] + q_r[n] = q^{(1)}[n], \tag{16}$$

where $q_\mathrm{b}[n]$ and $q_r[n]$ are the charge stored on $C_\mathrm{b}^{(\mathrm{e})}$ and $C_r = C_1$, respectively, whereas $q^{(1)}[n]$ is the charge transferred from the previous decimation stage.

On the next even clock cycle of $F_s^{(2)}$ denoted by ϕ_2, C_1 is disconnected from $C_\mathrm{b}^{(\mathrm{e})}$ for waiting the charge readout and discharged C_3 is connected to $C_\mathrm{b}^{(\mathrm{e})}$ for charge sharing resulting to a charge reduction of $q_\mathrm{t}[n]$ by a fraction $a_1^{(2)} = C_r/(C_r + C_\mathrm{b})$. At the same time, a new charge is transferred to parallel capacitors, therefore, the total charge stored on $C_\mathrm{b}^{(\mathrm{e})}$ and $C_r = C_3$ after the second even sampling instant is expressible as

$$q_\mathrm{t}[n+2] = (1 - a_1^{(2)}) q_\mathrm{t}[n] + q^{(1)}[n+2]. \tag{17}$$

Similarly, on ϕ_4, C_3 is disconnected from $C_\mathrm{b}^{(\mathrm{e})}$ and C_5 is connected to $C_\mathrm{b}^{(\mathrm{e})}$ for charge sharing. After transferring charge to $C_\mathrm{b}^{(\mathrm{e})}$ and C_5, the cycle is restarted at the next even period by transferring the charge again to parallel $C_\mathrm{b}^{(\mathrm{e})}$ and C_1.

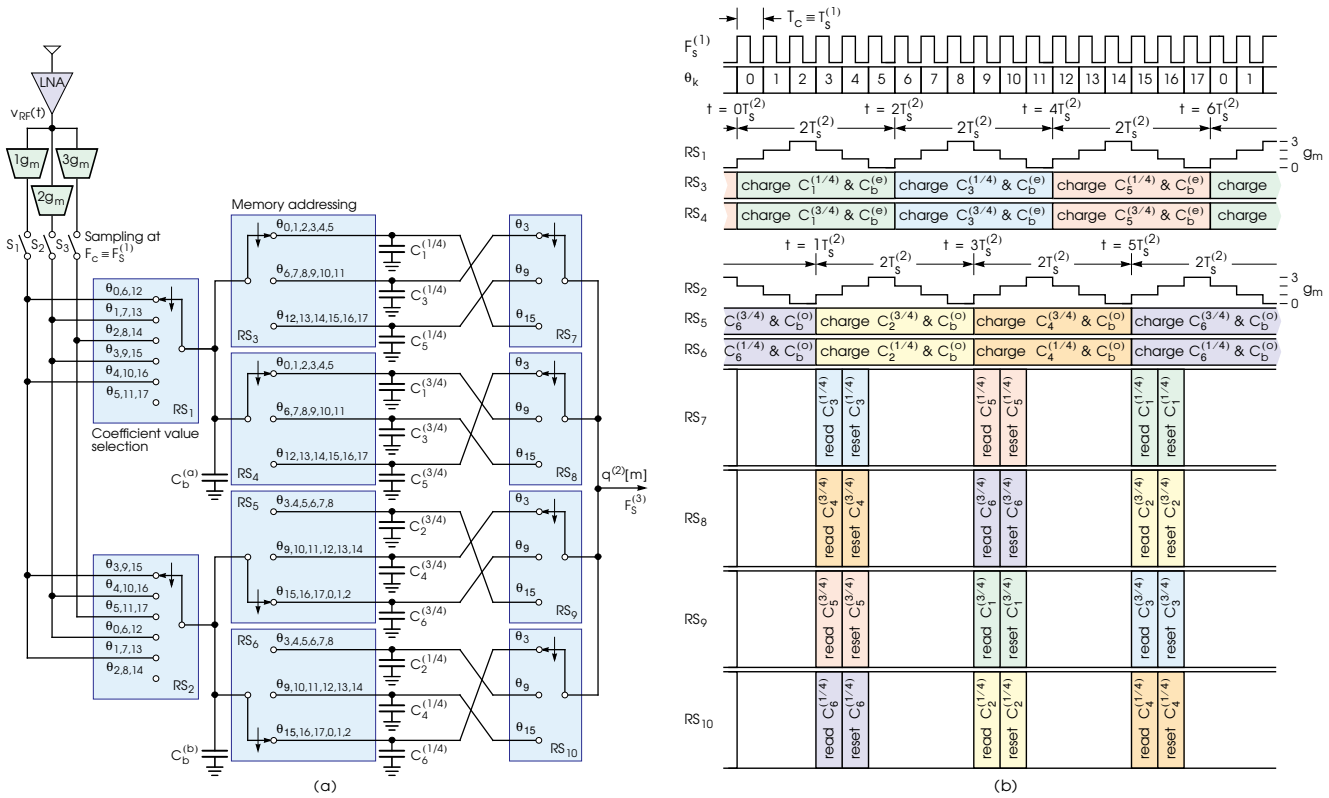

Fig. 8. (a) Charge-domain commutator-switch model of the time-interleaved combination of two first analog discrete-time decimation stages for *Case A* design. (b) A timing diagram.

The behavior of this model on the odd clock cycles is the same except that the charge processing is carried out using $C_{\mathrm{b}}^{(\mathrm{o})}$ and C_r for $r = 2, 4, 6$ instead of $C_{\mathrm{b}}^{(\mathrm{e})}$ and C_r for $r = 1, 3, 5$. The transfer function resulting from the charge sharing with the feedback capacitors $C_{\mathrm{b}}^{(\mathrm{e})}$ and $C_{\mathrm{b}}^{(\mathrm{o})}$ is given by (6a) with $S_2^{(1)} = 2$. This is due to the even/odd processing and the fact that the charge transferred by the feedforward capacitors is $a_1^{(2)} q_{\mathrm{t}}[n]$.

The charge stored on feedforward capacitors $C_r = C_r^{(1/4)} + C_r^{(3/4)}$ for $r = 1, 2, \ldots, 6$ are transferred to subsequent stage through commutators $\mathrm{RS_r}$ for $r = 7, 8, 9, 10$ such that for each even clock cycle either $C_1^{(1/4)}$, $C_2^{(3/4)}$, $C_3^{(3/4)}$, and $C_4^{(1/4)}$; $C_3^{(1/4)}$, $C_4^{(3/4)}$, $C_5^{(3/4)}$, and $C_6^{(1/4)}$; or $C_5^{(1/4)}$, $C_6^{(3/4)}$, $C_1^{(3/4)}$, and $C_2^{(1/4)}$ is connected to output. In this case, the output is the weighted sum of the charge corresponding to $q_{\mathrm{t}}[n]$ on the four most recent clock cycles at the rate of $F_s^{(3)} = F_s^{(2)}/2$ as given by

$$q^{(2)}[m] = \frac{1}{4}\Big(q_{\mathrm{t}}[n] + 3q_{\mathrm{t}}[n-1] + 3q_{\mathrm{t}}[n-2] + q_{\mathrm{t}}[n-3]\Big). \tag{18}$$

The overall frequency response for the second stage can be expressed as

$$H_2(\mathrm{e}^{\mathrm{j}2\pi f T_s^{(2)}}) = G_2^{(1)}(\mathrm{e}^{\mathrm{j}2\pi f T_s^{(2)}}) F_2^{(1)}(\mathrm{e}^{\mathrm{j}2\pi f T_s^{(2)}}), \tag{19}$$

where $G_2^{(1)}(\mathrm{e}^{\mathrm{j}2\pi f T_s^{(2)}})$ is the response due to charge feedback through capacitors $C_{\mathrm{b}}^{(\mathrm{e})}$ and $C_{\mathrm{b}}^{(\mathrm{o})}$ whereas $F_2^{(1)}(\mathrm{e}^{\mathrm{j}2\pi f T_s^{(2)}})$ is the frequency response of the second FIR anti-aliasing filter resulting from the summation of four samples weighted by the capacitance ratio. The desired value of $a_1^{(2)} = -b_2^{(2)} = 0.2$ for *Case A* design is achieved by choosing $C_{\mathrm{b}}^{(\mathrm{e})} = C_{\mathrm{b}}^{(\mathrm{o})} = C_r$. For *Case B* design, $a_1^{(2)} = -b_2^{(2)} = 0.8$ is achieved by selecting $C_{\mathrm{b}}^{(\mathrm{e})} = C_{\mathrm{b}}^{(\mathrm{o})} = 16C_r$.

For the final model these two first decimation stages can combined to form a highly efficient overall system as shown in Fig. 8. In this model, C_r for $r = 1, 2, \ldots, 6$ in Fig. 6(a) and Fig. 7(a) are merged to reduce the overall implementation cost. The decimation factors and the selectivity of the substages can still easily be modified by changing the transconductances as well as the values of the capacitors resulting in a flexible overall model.

C. Third Decimation Stage

The charge-domain model of the first FIR substage of the third decimation stage is shown in Fig. 9(a). This model corresponds to the transfer function $F_3^{(n)}(z) = 1 + z^{-1}$ for $n = 1$ in (12b) or (12e). The timing diagram for this model is depicted in Fig. 9(b). In this case, C_r for $r = 1, 2, 3, 4$ are charged through $\mathrm{RS}_{1,3,5,7}$ for the four consecutive clock of ϕ_n for $n = 0, 1, 2, 3$ such that when $F_s^{(3)}$ is high the charge from the previous stage is transferred into parallel C_1 and C_2; C_2 and C_3; C_3 and C_4; and C_4 and C_1, respectively. The charges stored into C_r's are read out such that on even clock cycles of ϕ_n when $F_s^{(3)}$ is low C_2 and C_4 are connected to output whereas C_1 and C_2 are connected to output on odd clock cycles. As a consequence, the charge at the filter output corresponds to the sum of the input charges of two consecutive clock cycles. The implementation of the $F_3^{(2)} = 1 + z^{-2}$ is the same, except two

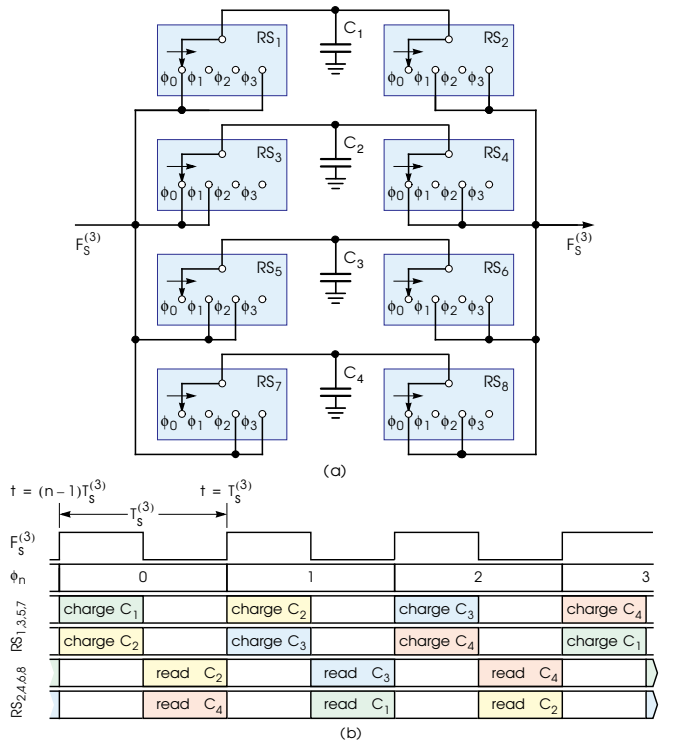

Fig. 9. (a) Charge-domain commutator-switch models of two first FIR substages of the third decimation stage for *Case A* design. (b) A timing diagram.

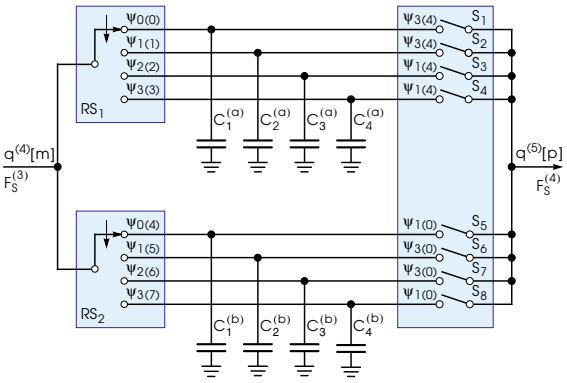

Fig. 10. Charge-domain commutator-switch model of the third non-recursive part of the third decimation stage for both *Case A* ($N_2 = 2$ and $K_2 = 2$) and *Case B* ($N_2 = 4$ and $K_2 = 1$) designs.

more capacitors are needed and the charging-readout process is carried out over six clock cycles.

The last substage of the non-recursive part of the third stage is depicted in Fig. 10(a). The behavior of this model is similar to non-recursive filter proposed in Subsection V-B except this model operates in two modes depending on the clock signals. These clock signals define both the decimation factor and the transfer function of the model.

For *Case A* design, $C_r = C_r^{(a)} + C_r^{(b)}$ for $r = 1, 2, 3, 4$ are charged through RS_1 and RS_2 such that the charge is transferred into C_r for $r = 1, 2, 3, 4$ on ψ_r for $r = 0, 1, 2, 3$, respectively. This charging scheme is repeated for the forthcoming clock cycles. The charges stored into the C_r's are read on every odd clock cycles of $F_s^{(3)}$ such that either $C_1^{(b)}$, $C_4^{(b)}$, and $C_3^{(a)}$ or $C_3^{(b)}$, $C_2^{(a)}$, $C_2^{(b)}$, and $C_1^{(b)}$ are connected to output. In this case, the output corresponds to the weighted sum of input charges stored during the three most recent clock cycles as expressed by

$$q^{(4)}[p] = q^{(3)}[m] + 2q^{(3)}[m-1] + q^{(3)}[m-2]. \quad (20)$$

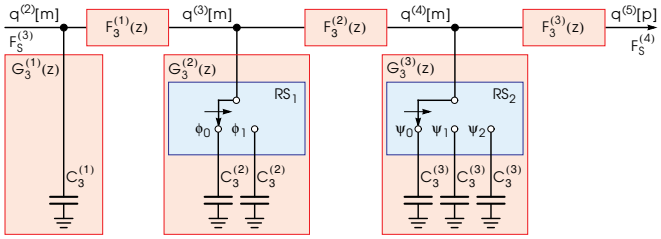

Fig. 11. Charge-domain commutator-switch models of three IIR substages of the third decimation stage for both *Case A* and *Case B* designs.

For *Case B* design, the C_r's are charged such that the charge is first transferred into $C_r^{(a)}$ for $r = 1, 2, 3, 4$ on ψ_r for $r = 0, 1, 2, 3$, respectively, and then into $C_r^{(b)}$ for $r = 1, 2, 3, 4$ on ψ_r for $r = 4, 5, 6, 7$, respectively. Again, this cycle is repeated for the forthcoming samples. In this case, the charge is read on every fourth clock cycles of $F_s^{(3)}$ such that either $C_1^{(a)}$, $C_2^{(a)}$, $C_3^{(a)}$, and $C_4^{(a)}$ or $C_1^{(b)}$, $C_2^{(b)}$, $C_3^{(b)}$, and $C_4^{(b)}$ are connected to output. This corresponds to the sum of the input charges over the past four clock cycles as given by

$$q^{(4)}[p] = q^{(3)}[m] + q^{(3)}[m-1] + q^{(3)}[m-2] + q^{(3)}[m-3]. \quad (21)$$

The recursive transfer functions $G_3^{(n)}(z)$ for $n = 1, 2, 3$ can be implemented in charge domain by connecting the feedback capacitors $C_3^{(n)}$ for $n = 1, 2, 3$ in front of the non-recursive subfilters as shown in Fig. 11. The first feedback capacitor, $C_3^{(1)}$, is charged at the same time as the capacitors in $F_3^{(1)}(z)$, however, $C_3^{(1)}$ is never discharged and, therefore, it realizes a first-order recursive filter due to charge feedback as the feedback capacitors in Section V-B. The next two feedback capacitors $C_3^{(2)}$ are charged such that the first capacitor is charged on every even clock cycle of $F_s^{(3)}$ and the second is charged on odd cycles. Again, the capacitors are never discharged, therefore, they realize a recursive transfer function. However, since they are charged alternately, the realized frequency response is periodic on baseband with the period of two. Similarly, the last three feedback capacitors $C_3^{(3)}$ are charged alternately on every third clock cycle and, consequently, the frequency response has a period of three.

The overall frequency response for the third stage can be expressed as

$$H_3(e^{j2\pi f T_s^{(3)}}) = G_3(e^{j2\pi f T_s^{(3)}}) F_3(e^{j2\pi f T_s^{(3)}}), \quad (22)$$

where $G_3(e^{j2\pi f T_s^{(3)}})$ is the response due to charge feedback through capacitors $C_3^{(1)}$, $C_3^{(2)}$, and $C_3^{(3)}$, whereas $F_3(e^{j2\pi f T_s^{(3)}})$ is the frequency response resulting from the summation of charges.

For the cascade implementation of $F_3(z)$ for *Case A* design, the sum of the unit capacitors needed to implement all the

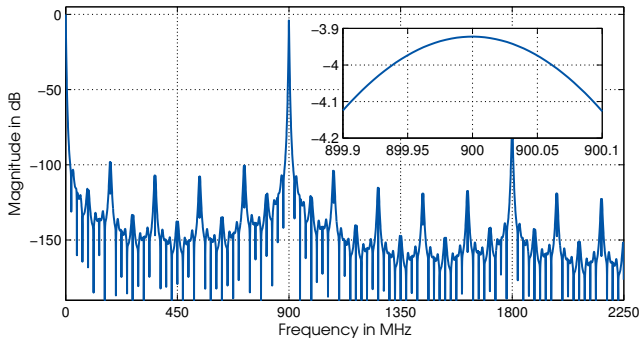

Fig. 13. Magnitude response of the overall decimator for *Case B* design.

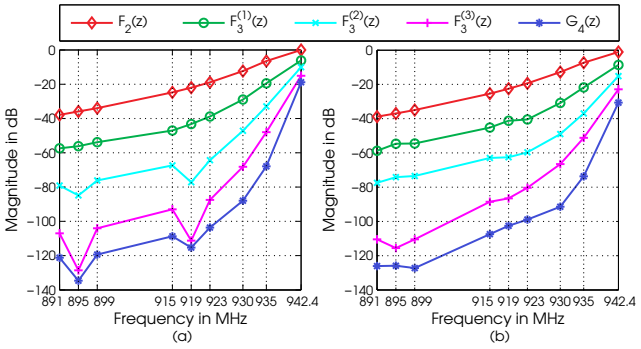

Fig. 14. Signal magnitudes at the output of the filter stages for several discrete frequencies with F_c = 942.5 MHz. (a) Ideal switches. (b) Switches with on and off resistance of R_{ON} = 5 kΩ and R_{OFF} = 100 MΩ, respectively.

$F_3^{(k)}(z)$ for $k = 1, 2, 3$ is 16. For the corresponding direct implementation, as given by,

$$F_3(z) = (1 + z^{-1})^4 = 1 + 4z^{-1} + 6z^{-2} + 4z^{-3} + z^{-4} \qquad (23)$$

the corresponding sum is 48 due to the time-interleaving required, that is, for the cascade implementation the number of unit capacitors is reduced by 67 percent. In addition, the cascade implementation typically reduces the sensitivity to component variations.

D. Last Filtering Stage

This structure is based on the passive switched-capacitor filter proposed in [14]. For the proposed design, this structure shares the charges with the previous subfilter. Therefore, the charge sharing has to be taken into account when evaluating the overall transfer function of this structure.

The transfer function of this second-order all-pole filter is given by (6b) where $a_4^{(1)} = \alpha$, $b_4^{(1)} = \alpha + \beta + \delta - 2$, and $c_4^{(1)} = (1 - \delta) + (\beta - 1)\alpha + (\alpha + \delta - 1)\beta$ with (cf. $G_4(z)$ in Fig. 12) $\alpha = C_{\mathrm{b2}}/(C_{\mathrm{i}} + C_{\mathrm{b1}} + C_{\mathrm{b2}})$, $\beta = C_{\mathrm{b2}}/(C_{\mathrm{b2}} + C_{\mathrm{h}})$, and $\delta = C_{\mathrm{i}}/(C_{\mathrm{i}} + C_{\mathrm{b1}} + C_{\mathrm{b2}})$. The values of $C_{\mathrm{b2}}^{(\mathrm{a})}$ and $C_{\mathrm{b2}}^{(\mathrm{b})}$ in Fig. 12 are equal, that is, $C_{\mathrm{b2}}^{(\mathrm{a})} = C_{\mathrm{b2}}^{(\mathrm{b})} = C_{\mathrm{b2}}$.

VI. Simulation Results

The simplified transistor-level implementation of the charge-domain sampler with embedded two first filtering stages as well as that of the two following stages is illustrated in Fig. 12. The overall implementation requires only 42 capacitors whereas the number of switches is 152 when including the number of switches used for resetting the capacitors. The ratio between the largest and smallest values of the capacitors in Fig. 12 are 9 and 16 for *Case A* and *Case B* designs, respectively, whereas the total number of unit capacitors needed to implement the overall design is 102. These figures illustrate fairly well the simplicity of the overall implementation even though they are based on the ideal switched-capacitor model.

Figure 13 shows for *Case B* design the simulated magnitude response of the overall decimator as well as the passband details. This simulation is carried out by using a discrete-time switched-capacitor simulator written in MATLAB. The magnitude response is determined by driving the input with a single sinusoidal and then measuring the signal magnitude at the output. For this design, the response is evaluated using 3 200 equispaced discrete input frequencies on $[0, 2.5F_c]$ and 16 discrete frequencies on $[F_c - f_p, F_c + f_p]$.

When realizing switched capacitor circuits, the matching properties of the capacitors are of great importance since the performance of the circuit is determined by the capacitance ratios. Typically the matching error between two or more capacitors is minimized by constructing the capacitors using a bank of identical unit capacitors connected in parallel. Combined with a careful layout design, this technique can provide an accuracy of 0.1 percent in capacitance ratios [17]. The sensitivity analysis for the proposed design was carried out using Monte Carlo simulations with 500 interations. The component values to be varied were set to random values drawn from a uniform distribution centered around the ideal value. The accuracy of the components were set to 0.1 percent. The sensitivity analysis to tolerances in component values show the combined attenuation of the decimator architecture and the commericial duplex filter well exceeds the required attenuation characteristic.

Figure 14 shows the simulated signal magnitudes at the output of $F_2(z)$, $F_3^{(n)}(z)$ for $n = 1, 2, 3$, and $G_4(z)$ for *Case B* design with nearly ideal swithes and swithes with nonideal characteristics. These simulations were carried out using transient analysis in SPICE simulator. The values are scaled such that the dc-gain of the signal with the largest magnitude is equal to 0 dB. As seen from this figure, the nonideality of the switches both reduces the signal levels as well as degrades the selectivity. However, this reduction of signal levels can be compensated if needed by adding simple low-gain amplifiers between subsequent sections as described in [16] whereas the loss of selectivity can be compensated by either increasing the values of the feedback capacitors or the number of stages.

VII. Conclusions

A fully reconfigurable architecture is proposed for multistandard receiver front-end. This architecture is based on bandpass sampling and analog discrete-time signal processing. The proposed architecture can be adapted to several desired wireless standands by simply adjusting the input sampling rate and the clocking scheme of the switched capacitors.

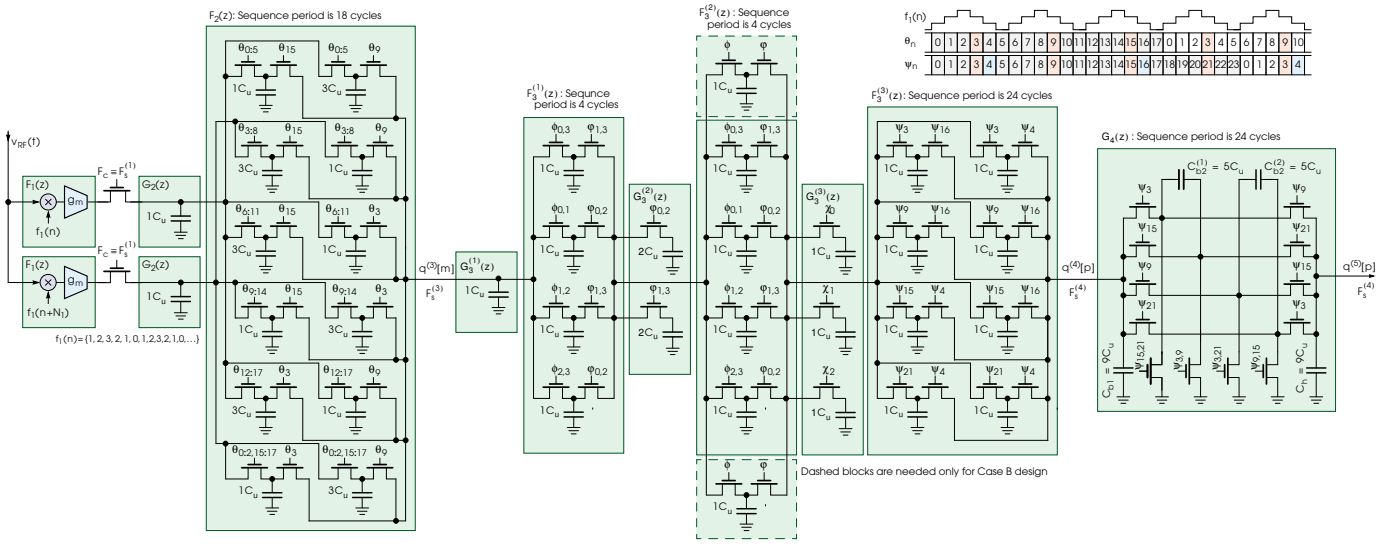

Fig. 12. Simplified transistor-level implementation of the overall system for both *Case A* and *Case B* designs. For simplicity, the clock signals are depicted only for *Case A* design.

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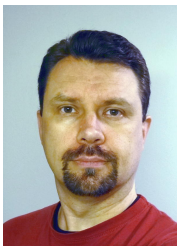

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