MULTIRATE DIGITAL FILTER DESIGN FOR A PAL TV MODULATOR

Juha Yli-Kaakinen, Ming Hu, Riku Uusikartano, Teemu Kupiainen, and Markku Renfors

***Abstract*—This paper develops a multirate digital filter design for the Vestigial SideBand (VSB) modulator required in the analog TV transmission systems, like PAL. The modulator takes as the input the composite video signal digitized at 13.5 MHz sample rate and the output is a VSB signal modulated to the usual 38.9 MHz IF picture carrier frequency and sampled at 121.5 MHz rate. The design is based on a complex baseband VSB filter running at the input sampling rate, digital multirate techniques for increasing the sampling rate by the factor of nine, and a combination of multirate techniques and digital mixing to translate the signal to the 38.9 MHz picture carrier frequency.**

***Index Terms*—PAL modulator, VSB filter, multiplierless design.**

I. INTRODUCTION

THE traditional analog TV transmission systems have still a lifetime of many years, even though the new digital transmission techniques are being taken into use. In this situation, there is interest to more advanced implementation techniques for the traditional analog systems. The fast development of digital signal processing techniques allows to process analog signals with greater flexibility, reliability, and lower costs. For example, in CATV networks, the incoming TV signals are in many cases in digital format and also the modulators for new digital standards are using digital signal processing all the way to the IF stage. In this situation, it would be advantageous to be able to perform the analog TV modulation using digital signal processing techniques.

In this paper we develop a PAL modulator based entirely on digital signal processing techniques. The input signal is assumed to be a composite baseband video signal (i.e., it includes both the baseband luminance component and the chrominance components modulated to the color subcarrier) with 13.5 MHz sampling rate. Further, it is assumed that the input video signal is bandlimited from the low frequency end in such a way that there are no signal components which would disturb the audio carriers to be included in the complete TV signal. Therefore, there is no need to implement the lower stopband part (below -5.5 MHz) of the specifications [1] here. This means also that the audio components could be included in the signal already before the VSB filter. A suitable digital implementation of an audio modulator is described in [2]. Amplitude and group delay response specifications for the PAL B/G system are depicted in Fig. 1.

The proposed design is based on low-order recursive Nth-band filters [3], [4] and Hilbert-transformer sections [5], [6], which are found to be very efficient in sampling-rate conversion applications [7]. The allpass subfilters are basic building blocks for these filters. The different filter types composed of allpass filters are characterized by many attractive properties, such as a reasonably low coefficient sensitivity, a low roundoff noise level, and the absence of parasitic oscillations. In addition, these allpass subfilters can be realized by using first- and second-order allpass sections as building blocks. Therefore, the resulting structures are highly modular which makes them suitable for signal processor and VLSI implementation.

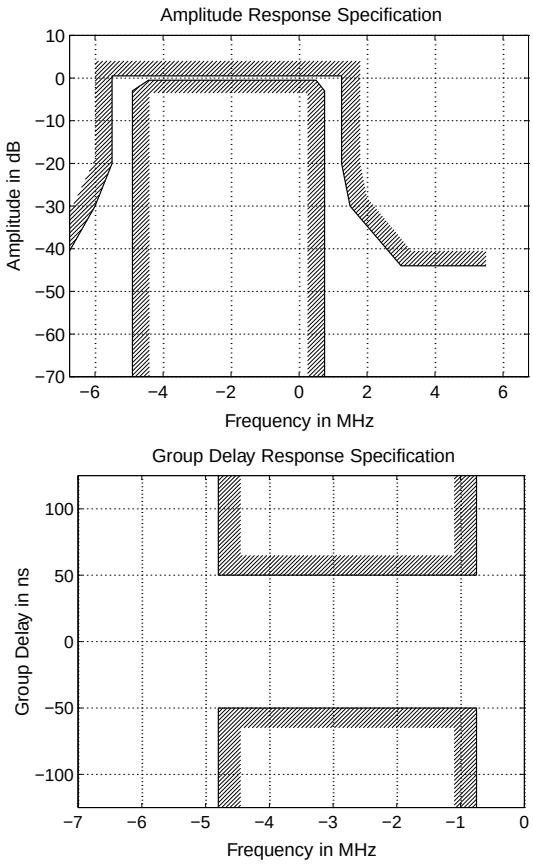

Fig. 1. Amplitude and group delay response specifications for the VSB filter for PAL system.

It is also possible to design recursive Nth-band filters to have an approximately linear phase in the passband by selecting the one of the allpass subfilters to consist of pure delay elements [4], [5]. Such designs are especially suitable for applications where linear-phase finite impulse response (FIR) filters would have an excessive signal delay.

In highly customized VLSI implementations, a general multiplier is very costly. Therefore, it is attractive to carry out the multiplication of a data sample by a filter coefficient using a sequence of shifts and adds [8], [9]. The shifts are often hardwired and hence they are essentially free. Thus, only a few

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Manuscript received June 28, 1999

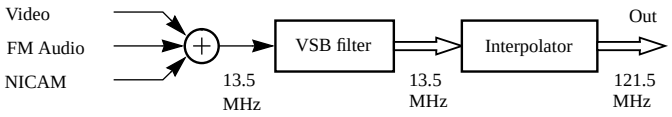

Fig. 2. Digital VSB modulator.

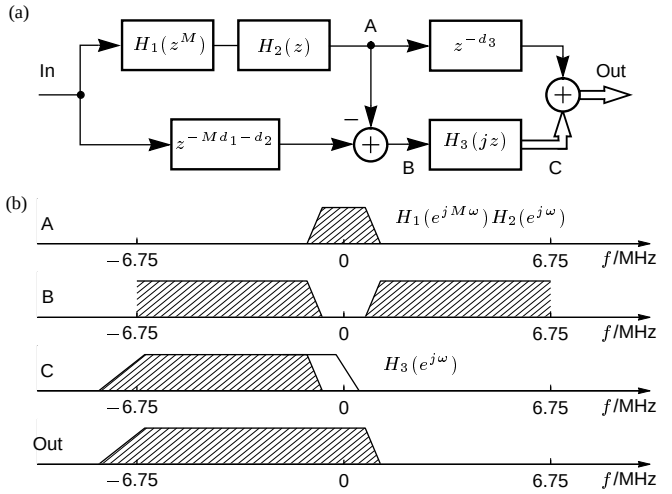

Fig. 3. The proposed VSB filter structure. (a) The overall structure. (b) Characteristic amplitude responses of the subfilters.

adders or subtracters are required for each coefficient of the filter. This leads to a significant reduction in computational complexity, power consumption, and silicon area. The PAL modulator design has been optimized in order to be able to use as simple filter coefficients as possible. The resulting design is quite feasible for implementation as an ASIC or even on an FPGA circuit.

The outline of this paper is as follows. Section II of this paper introduces the overall structure of the VSB modulator. The VSB filter stage of the baseband PAL modulator is briefly described in Section III. In Section IV, the efficient implementation of the interpolator and mixing section is considered in detail. ASIC implementation of the VSB-filter is described in Section V. Finally, the conclusions are given in Section VI.

II. Overall Structure

Figure 2 shows the overall block diagram of the proposed VSB modulator. The A/D-converted composite video signal and the audio components are first combined and fed to the VSB filter which partially suppresses the positive frequency part of the input signal. The DC-level of the input signal can be used to control the residual carrier level. After the VSB filtering the signal consist of the in-phase (I) and quadrature (Q) components. The I/Q signal then passes through the interpolation and mixing section, which increases the sampling rate by the factor of nine using multirate filtering. In addition, the signal is simultaneously translated in the frequency domain to the usual 38.9 MHz picture carrier frequency by using two simple numerically controlled oscillators (NCO's) in combination with multirate techniques.

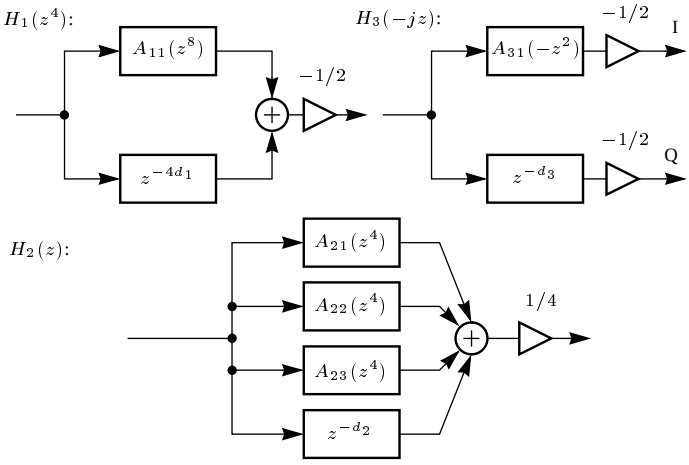

Fig. 4. Subfilter structures of the VSB filter based on approximately linear-phase Nth-band filters.

III. VSB Filter

The VSB filter is implemented as a complex baseband filter, which is quite feasible in case of digital signal processing, even though the analog VSB filtering is normally carried out at the IF stage. Figure 3 shows the structure of the multi-stage VSB filter, which is described in more details in [10]. The characteristic amplitude responses at the different stages of the VSB filter are also shown in Fig. 3. Notice that only the output of the filter is complex, all other parts are implemented using real signals.

The design is based on low-order infinite impulse response (IIR) Nth-band filter and Hilbert-transformer sections, as shown in Fig. 4. Digital allpass filter sections are the basic building blocks of all these filters. In order to satisfy the strict group delay response specifications [1], the approximately linear-phase IIR Nth-band filters are utilized. The required filter orders for the allpass sections are:

- $H_1(z)$, $H_3(z)$: branch 1 is a 4th-order allpass; branch 2 is a pure delay
- $H_2(z)$: branches 1, 2, and 3 are 2nd-order allpasses, branch 4 is a pure delay.

The filter coefficients have been optimized utilizing techniques described in [9]. Considering the sums of powers-of-two coefficient representation, the number of adders needed to implement all the filter coefficients is nine. The magnitude response of the VSB filter as well as the passband details of the group delay are shown in Fig. 5.

IV. Interpolator Design

The other sections of the VSB modulator increase the sampling rate by a factor of nine to 121.5 MHz and translate the signal to the 38.9 MHz picture carrier frequency, using the block diagram shown in Fig. 6. The interpolation is also carried out by using IIR Nth-band filters. The frequency translation is done partly through the imaging effect of the multirate signal processing, and partly through the frequency translation by digital I/Q-mixing.

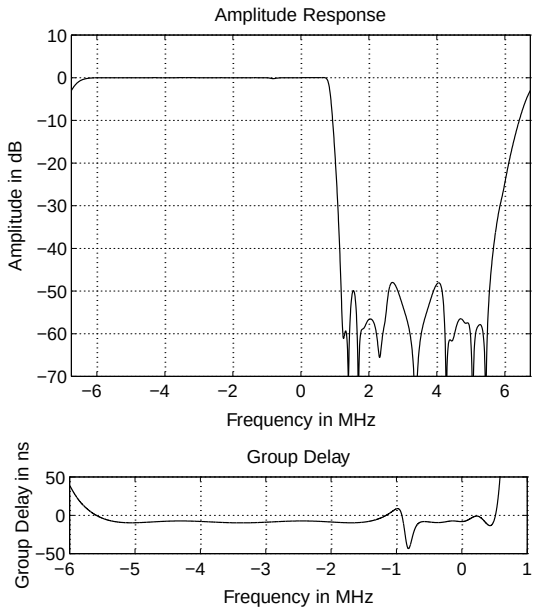

Fig. 5. Amplitude and group delay responses for the optimized design.

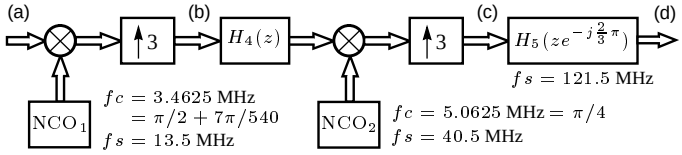

Fig. 6. Block diagram for the interpolation and mixing section.

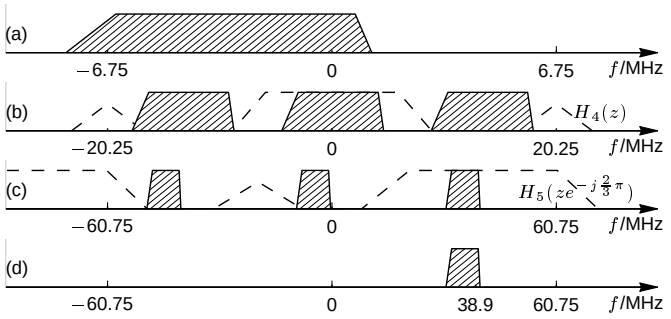

Fig. 7. Characteristic amplitude responses at the different stages of the interpolation and mixing section.

A. Interpolation and Mixing Algorithm

The structure of the PAL modulator is designed to minimize the computational and hardware complexity. By implementing the interpolation at two stages, the requirements for the anti-imaging filters can be dramatically reduced. In addition, the multistage approach is preferred because part of the filtering can be performed at the lower sample rate. This results in a significant reduction in overall hardware complexity and multiplication rate as compared to general single-stage approach [3].

The two-stage interpolation and mixing process is illustrated in Fig. 7. At the first stage, the output of the VSB filter, as shown in Fig. 7(a), is transformed to a nearly symmetric baseband signal using digital I/Q-mixing. After the first interpolation by three, the undesired images of the signal are attenuated using 3rd-band filter $H_4(z)$ which has the magnitude response represented by the dashed line in Fig. 7(b). At the second stage, the signal is upconverted by multiplying it with $e^{j\pi k/4}$ and the sampling rate is further increased by three. The resulting signal is filtered by $H_5(ze^{-j\frac{2}{3}\pi})$ which is the $f_s/6$-shifted version of the normal 3rd-band filter. This is done for attenuating the undesirable images. Figure 7(c) shows the spectrum of the interpolated signal as well as the amplitude response of $H_5(ze^{-j\frac{2}{3}\pi})$. As a result, we have a VSB signal modulated to 38.9 MHz and sampled at 121.5 MHz as shown in Fig. 7(d).

B. Interpolation Filter Design

Approximately linear-phase IIR Nth-band filters are also used for the interpolation filtering due to the group delay specifications [1]. In order to satisfy the adjacent channel rejection specifications, the stopband attenuation requirements for the anti-imaging filters $H_4(z)$ and $H_5(ze^{-j\frac{2}{3}\pi})$ are approximately 58 dB.

The minimum number of coefficients for $H_4(z)$ to meet the amplitude criteria is six. However, to allow some margin for the coefficient quantization, it has to be increased to eight. The required orders for the allpass sections are: branches 1 and 2 are 4th-order allpasses; branch 3 is a pure delay. For $H_5(ze^{-j\frac{2}{3}\pi})$, the specifications are fulfilled using only four coefficients. In this case, branches 1 and 2 are 2nd-order allpasses and branch 3 is a pure delay.

Again, the coefficients of the allpass subfilters were optimized such that the overall filter satisfies the given amplitude criteria with the simplest coefficient representation forms. The optimization algorithm is based on the observation that by first finding the largest and smallest values for both the radius and the angle of all the complex-conjugate poles as well as the largest and smallest values for the radius of a possible real pole in such a way that the given criteria are still met, we are able to find a parameter space which includes the feasible space where the filter specifications are satisfied. After finding this larger space, all what is needed is to check whether in this space there exist desired discrete values for the coefficient representations [9].

Considering the sums of powers-of-two coefficient representation, a total of only five adders are required to implement all the filter coefficients for $H_4(z)$. In this case, seven fractional bit are required to meet the specifications. For $H_5(ze^{-j\frac{2}{3}\pi})$ the criteria are met using also five adders. In this case, only six fractional bits are needed. Figure 8 shows the magnitude response as well as the passband details of the overall system.

When we are using adaptors shown in Fig. 2(a) in [11], to implement the branch filters, the number of additions required for the adaptor implementation is 36. It should be pointed out that the number of adders may be further reduced by using other allpass filter structures (see, e.g., [12], [13]).

The interpolation filtering may be implemented very efficiently using alternating switches, or commutative structures, as shown in Fig. 9. In this case, each of the subfilters is operating at the lower sample rate. This reduces the computational complexity per input sample remarkably. In case of $H_5(ze^{-j\frac{2}{3}\pi})$ only the I output is shown, in which case the overall system has real

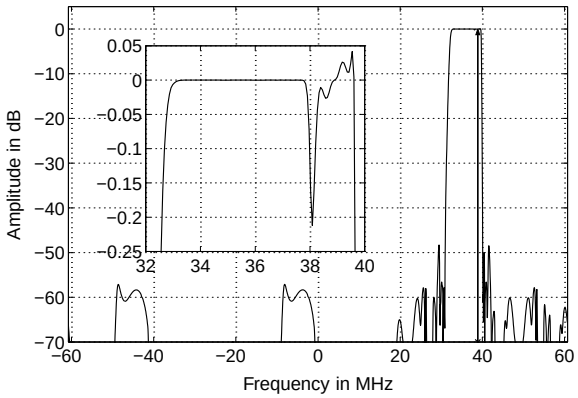

Fig. 8. Amplitude response for the overall design.

output with symmetric spectrum. If complex output is desired, then the structure has to be duplicated with some modifications for the Q output.

C. Numerically Controlled Oscillator

The system has been optimized in order to be able to use as simple NCO's as possible for generating the digital local oscillator signals.

The first NCO can be implemented using the techniques presented in [14]–[17]. Since the oscillator's output frequency is fixed and has a rather simple fractional relation to the sampling rate, the phase accumulator and the sine/cosine ROM can be optimized quite efficiently.

The second NCO's sampling rate is eight times the output frequency. This results in oscillator samples of $\cos(n\pi/4)$ and $\sin(n\pi/4)$ which have the values 0, $\pi/2$, 1, $\pi/2$, 0, $-\pi/2$, -1, $-\pi/2$, $0, \cdots$. Therefore, the function of the NCO and the mixer can be implemented with two constant coefficient multipliers and some multiplexers and complementers.

Further reduction is obtained by sharing a single multiplier by both the I and Q rails. This is done by inserting a pipeline register in the I channel before the mixer and in the Q channel after the mixer. A multiplier with 12-bit coefficient precision can be realized with only three adders.

V. ASIC Implementation

As shown in Figs. 3 and 4, the VSB filter is constructed by using delay elements and first- and second-order allpass sections. Since the coefficients for the first- and second-order allpass sections are optimized as simple combinations of powers of two, a multiplication for each coefficient of the filter can be realized by a few simple shift operations and adders/subtracters.

The hardware description language VHDL was used to model hierarchically the designed VSB filter. Additional pipeline registers were inserted to the filter structure in Fig. 3 based on some estimations.

Parallel computational style was used for design simplicity. Positive edge-triggered static master-slave D flip-flops were used for delay elements for their robustness and ripple carry adders were used for their small area and regularity.

The VHDL model simulation results were compared with MATLAB simulation results to verify the performance of the designed circuits and to determine the additional bits needed to satisfy finite wordlength effects. In order to avoid overflow and to satisfy round-off noise requirements, three more additional bits are needed when input is 13 bits sinusoidal test signal. Using 16 bit overall data wordlength (12 fractional bits, 3 integer bits and sign bit) in internal computations, the round-off noise level is well over 60 dB below the picture-carrier level of the PAL-modulated signal.

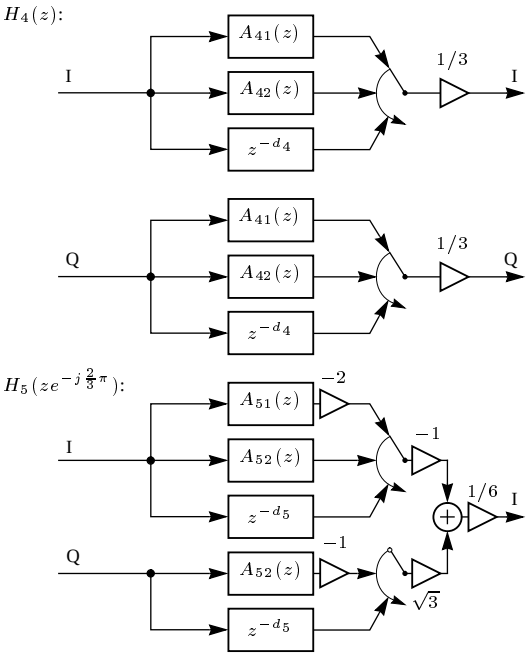

Fig. 9. Interpolation filter structures.

The VHDL model was synthesized for a 0.35 μm technology [18] . The synthesis results are summarized in Table I.

VI. Conclusions

We have developed a VSB modulator design for the PAL specifications utilizing entirely digital signal processing. The design is based on low-order allpass filter sections and two

TABLE I
SYNTHESIS RESULTS.

Data format	13-bit input and output 16-bit internal
Total area	2.6 mm^2
Layout density	14 000 gates/mm^2
Gate count	36 400
Operating clock frequency	13.5 MHz
Average power consumption	0.25 μW/MHz/gate
Power dissipation	123 mW at 13.5 MHz
Technology	0.35 μm, 3.3 V, 4-metal, n-well standard cell process

simple NCO's and I/Q mixers. The resulting design has significantly lower complexity than in the earlier designs using FIR filters [19], [20] and it is quite feasible for implementation as an ASIC or even on an FPGA circuit.

ACKNOWLEDGMENT

This work was carried out in the project "Digital and Analog Techniques for Flexible Receivers" funded by the Technology Development Center of Finland (Tekes), Teleste Ltd, and other companies.

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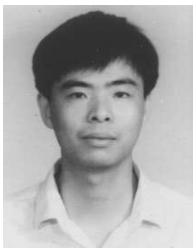

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