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DESIGN AND IMPLEMENTATION OF A LOW POWER FIR FILTER BANK

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ABSTRACT

We propose a low voltage low power (<250μW @1.1V, 1 MHz) FIR filter bank (excluding RAM) for hearing aid applications. The filter bank is composed of 16 non-uniform bands that are designed to imitate the frequency response of human ears. The filter bank covers the frequency range from 0 to 7.75 kHz and provides a stopband attenuation of 60 dB for each band. We achieve our low power attributes by four means. First, we propose to generate a set of decoded input signals and share the signals to all 16 bands. By means of multiplexers. Adder arrays and control logic, the decoded signals are added and accumulated for each bands, without requiring power-hungry multipliers. Second, we reduce the number of multiplications by half using folded cascade implementation (linear phase structure). Third, we truncate the two least significant bits of the filter coefficients and adopt 24-bit length (instead of 32-bit) for internal data bus to reduce the power dissipation without sacrificing much the performance of the filter bank. Finally, we use sign-magnitude representation for the filter coefficients to reduce the spurious switching (and hence lower power dissipation). The core of the filter bank occupies ~1.65mm^2 by using a 0.35μm dual poly four metal CMOS process. When compared to a conventional filter bank, we show that our design features low power dissipation (~50% lower for the filter bank core) for the same magnitude response.

INTRODUCTION

Some of the reasons for the popularity and prevalence of portable electronic devices include a reasonable lifespan of the remote power source (batteries) and sophistication of such devices. An example of such a device is the hearing instruments (hearing aids) where they are effectively used as assistive portable electronic medical devices to improve the speech intelligibility of the hearing impaired. In this application, its battery lifespan is expected to exceed 100 hours from a small pill-size battery (1.1V – 1.4V) with a typical energy capacity of 100mAh. The degree of sophistication of a device is essentially the amount of signal processing embodied within the devices. The amount of signal processing embodied in many portable devices is largely constrained by the amount of power drawn that can be tolerated, or equivalently the minimum lifespan of the battery.

In hearing instruments, the maximum current (not including the audio power output) tolerated is of the order of 1mA @ 1.1V-1.4V. In view of this tight power constraint, complex signal processing algorithms such as the highly desirable noise reduction

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algorithm [Sim, 1998] are not implemented in present-day hearing instruments (although highly simplified versions are sometimes implemented). Design methodologies for low power operation are well established and continue to attract much research [Chandrakasan, 1992]. These methodologies span from system-level design to transistor low- to medium-speed (1~2 MHz) power-efficient architectures, low power standard library cells with a small feature size fabrication process, power-efficient peripheral designs such as Class-D amplifier [Gwee, 2002] and ultra low power digital cell designs are perhaps more prevalent. In the case of the hearing instrument, all these techniques are already adopted.

In many audio applications, including hearing instruments, the filter bank is one of the major signal processing blocks and is often the block that dissipates the largest power. Figure 1 depicts the block diagram of a hearing aid that embodies a filter bank. In the frequency domain viewpoint, the filter bank decomposes the input signals into multiple sub-band signals or bands where the magnitude response of each band can be independently varied. The filter bank in many audio devices is used as the graphic equalizer to shape the magnitude of frequency response. In hearing instruments, the filter bank is not only used to shape the magnitude of the frequency response such that the amplification of the audio signals commensurate with the hearing impairment (according a prescription formula) but also is used in some noise reduction algorithms. In the hearing instrument industry, the ability to shape the magnitude response is often referred to as 'programmability'.

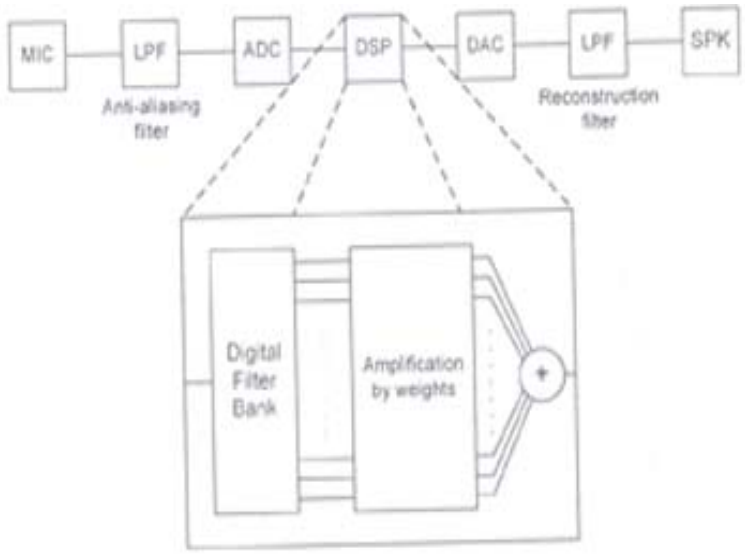

Figure 1: Block Diagram of a Digital Hearing Aid That Embodies a Filter Bank

In many designs, the filter bank typically comprises between 8-32 bands, where the filtering function of each band is typically a 4^{th} order Butterworth (Maximally Flat) filter. The higher number of bands (e.g. ≥16 bands) with better magnitude response (e.g. ≥50 dB stop attenuation for each band) the higher programmability of the filter bank. The

passband bandwidth of the bands of the filter bank, otherwise known as the filter bank spacing, may be uniform or non-uniform. Of the two filter bank spacings, the non-uniform filter bank is more desirable as the non-uniform bands can be adjusted, to a large extent, to better fit the physiological sensitivity of human hearing [Pohlmann, 2000]. Nevertheless, the cost of implementing either a very high programmability filter bank (≥16 bands with ≥50 dB stop attenuation per band) or a non-uniform filter bank is high (high computations) that in turns increases the total power dissipation of the circuit.

In this paper, we propose the design of a 16-bit 16-band lower power (~250μW @ 1.1V, 1.024 MHz) high performance (109 filter order with >60dB stopband attenuation per band) non-uniform FIR (Finite Impulse Response) filter bank for a digital hearing instrument; any number of bands can be designed and the 16-band example here simply serves as a delineation of the proposed methodology. The filter bank covers the frequency range from 0 to 7.75 kHz within ± 1 dB passband ripples using Kaiser window method. The adoption of the FIR structured design is for its phase stability (as opposed to IIR (Infinite Impulse Response) that features potentially phase instability) and its regular structure. We obtain our micropower filter bank by a set of multiplexers. The decoded input signals are then added signals for all 16 bands by a set of multiplexers. The decoded input signals are then added and accumulated by the adder arrays for each band. The sharing of the decoded input signal is novel in our filter bank design as we only require a set of shifters and adders and then 16 sets of Bank of Multiplexers and Adders to perform the multiplications for the proposed 16-band filter bank. It is different from the conventional approach where 16 multipliers are required – multipliers dissipate significant amount of power. Second, we further reduce the number of multiplications by half using the folded cascade implementation (linear phase structure). Third, we truncate two LSBs (least significant bits) of the filter coefficients and adopt 24-bit length for internal intermediate data bus (as opposed to 32-bit in conventional designs) without sacrificing much the performance of the filter bank. Finally, we employ the sign-magnitude representation (for its low switching activity property) for the filter coefficients.

We design and verify the magnitude response of our filter bank design by using Matlab. Based on a commercial 0.35μm CMOS digital standard library cells, we implement our filter bank using Verilog and synthesize our design using Synopsys Design Compiler. We then layout our IC prototype using Cadence Silicon Ensemble. On the basic of pre- and post-layout computer simulations, we verify our result and show that our design dissipates 50% lower power than the conventional filter bank design for the same magnitude response.

LITERATURE REVIEW ON FILTER BANK DESIGNS

In this section, we first specify our filter bank design and then briefly review the prevalent methods in low power filter bank designs. This review will provide a better perspective to our design in Section 3.

We list the frequency range of the individual 16 bands of the non-uniform filter bank and state the specifications of our filter bank design in Tables 1 and 2. In Table 1, we limit the upper frequency range to 7.75kHz. It is sufficient for speech. These 16 non-uniform frequency spacings of the filter bank are interpolated according to on the Bark Scale of known as critical band [Pohlmann, 2000]. In Table 2, we limit the power dissipation our filter bank design less than 500μW @ 1.1V, 1.024MHz. The low system clock rate (1.024 MHz) is for the low power dissipation considerations for the entire hearing aid device. As a result, the filter bank should complete the entire operations within 64 clock cycles for real-time considerations. Despite the low clock rate, we yet demand the magnitude response of the filter bank to at least >50dB for high programmability. We select linear phase implementation in our filter bank design due to its phase stability consideration. For aesthetics consideration, we also limit the core area of our filter bank to be less than 4 mm^2.

Table 1: Frequency Range for the 16 Non-uniform Bands

Proposed Critical Bands				
Band	**Lower Frequency (Hertz)**	**Center Frequency (Hertz)**	**Higher Frequency (Hertz)**	**Bandwidth (Hertz)**
1	0	123	246	246
2	246	369	492	246
3	492	615	738	246
4	738	861	984	246
5	984	1119	1254	270
6	1254	1402	1550	296
7	1550	1722	1894	344
8	1894	2078	2263	369
9	2263	2460	2657	394
10	2657	2890	3124	467
11	3124	3382	3641	517
12	3641	3936	4231	590
13	4231	4576	4920	689
14	4920	5314	5707	787
15	5707	6175	6642	935
16	6642	7196	7750	1108

Table 2: Specifications of the Filter Bank

	Specifications
Sampling Frequency	16kHz
System Clock Frequency	1.024MHz
Power Dissipation	<500μW @ 1.1V
Magnitude Response	>50 dB
Phase Response	Linear Phase
Core Area	< $4mm^2$

Many reported designs have been introduced for the low power filter bank designs. Nielsen and et. al. [Nielsen, 1999] proposed a 7-band asynchronous IFIR filter bank with filter coefficients containing at most 3 ones. Their design dissipated as low power as 85μW @ 1.55V. However, their design is limited by its poor programmability (only 7 bands with 40 dB attenuations). Tan and et. al. [Tan, 2001] designed a wave digital 16-band filter bank which employing a multiplexed bit-parallel approach and clock gating for low power dissipation. Nevertheless, their design still drew relatively high power as ~ 480μA @ 1.1V. Another approach is by limiting the number of ones in the filter coefficients that leads to a reduction in the number of computations, resulting in low power dissipation in the filters [Yli-Kaakinen, 2001]. This approach, from algorithmic views, always requires a lot of complex computer optimizations and verification for the filter bank design. More other literature on filter bank designs can be found in [Mitra, 2001].

As this outset, we do not consider the abovementioned designs for our comparison. This is due to the differences in the number of filter bands used and the amount of attenuation designed. For fair comparison, we implement a conventional FIR filter bank design (16 separate FIR filters) [Mitra, 2001] for the same magnitude response (see Table 1). The simulation results (our design and the conventional design) are then compared directly (see later) to demonstrate our proposed design features lower power dissipation.

PROPOSED ARCHITECTURE

In multiplication-intensive applications such as in FIR filters, it is desirable to reduce the amount of multiplications since multiplications are the major contributors of power consumption. In an equal bandwidth design, the coefficients of the filter bank can be optimized in such a way to reduce the number of multiplications while still maintaining regular filter structure [Nielsen, 1999]. As our specification is to design a critical-band-like hearing aid that fits better for human ears, the relationship among the coefficients is not straightforward and further optimization will make the filter bank structure irregular. This irregularity will in turns create some overheads in terms of hardware and computations which are not acceptable for low power design.

To circumvent this problem, we propose an algorithm with a novel architecture which will reduce the power dissipation during the multiplication process, regardless of the coefficients irregularity. Instead of using conventional multipliers to perform the multiplication, we use a Bank of Multiplexers and Adders (BMA).

The general architecture of the filter bank is shown in Figure 2.

We sample the input signal at the frequency of 16 kHz and store the data inside the memory (RAM). To implement linear phase structure [Mitra, 2001] for low multiplication considerations, at every clock cycle two input data are read from the memory and added together to form an intermediate data. This intermediate data will undergo a set of shifting and addition to provide the inputs for the BMA. As the input data is the same for all 16 bands, these inputs need to be calculated only once every clock

cycle. This greatly reduces the number of computations needed. As a result, our design requires only a set of shifters and adders and then 16 sets of BMA for each band. It is different from the conventional approach, 16 power-hungry multipliers are required.

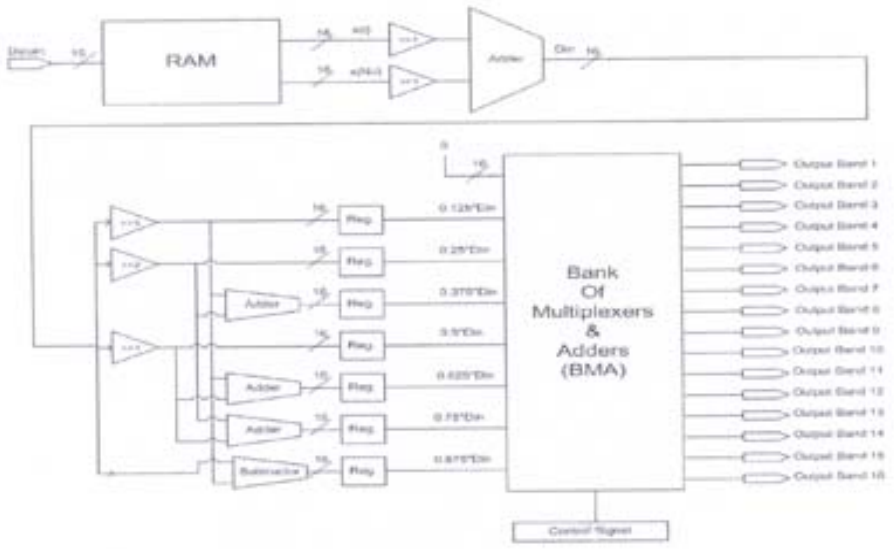

Figure 2: Proposed Filter Bank Arechitecture

Inside the BMA are the multiplexers and adders. For each band, three/four multiplexers and two/three adders are to replace a multiplier. Figure 3 shows the details block diagram of the BMA for the multiplication process for the 1st frequency band.

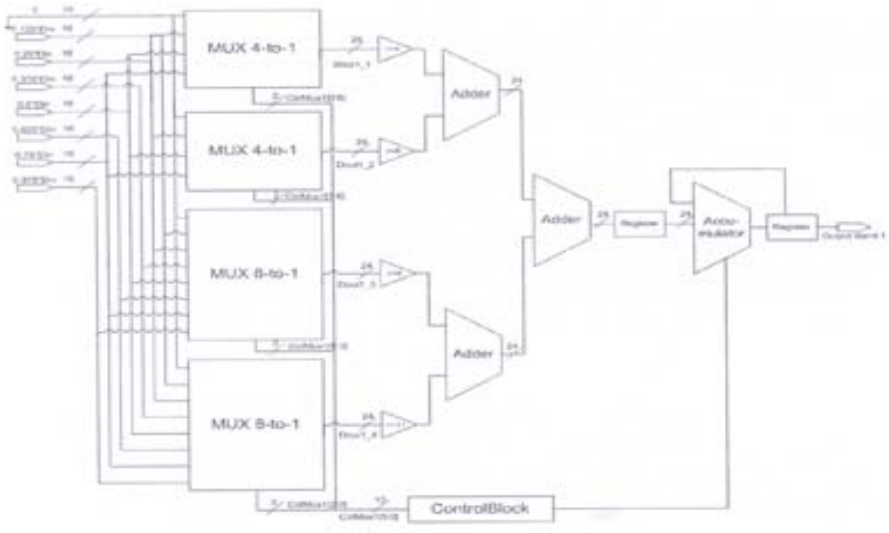

Figure 3: Block Diagram of the BMA for the 1st Frequency Band

At every clock cycle, the controller (ControlBlock) provides the select signals for the multiplexers. These select signals correspond to the filter coefficients for that frequency band. The outputs of the multiplexers are shifted accordingly before they are added together to form the multiplication result. The coefficients are represented in signed magnitude form such that the MSB (most significant bit) corresponds to the sign bit. The controller determines whether the accumulator will perform addition or substraction based on this MSB. After 64 clock cycles, we can obtain the output signal from the accumulator output.

For 16-bit input data and 16-bit coefficient multiplication, the resulting product is 32-bit. In our design, we only use the first 24 MSBs of the output (instead of 32-bit) as it gives the optimum trade-off between accuracy and power according to our investigation. The truncation of the internal data bus bit length (from 32-bit to 24-bit) has only a little effect on the quantization errors but reduces the power dissipation significantly. The final output of the filter bank remains 16-bit after completing the entire process.

RESULTS

We first design and simulate our filter bank using Matlab. All the frequency bands are designed so that they tolerate a maximum passband ripple within ±1.5 dB and minimum stopband attenuation of 60 dB. These frequency bands are realized using Kaiser Window method with a filter order of 109. Figure 4 shows the frequency responses of the 16 frequency bands.

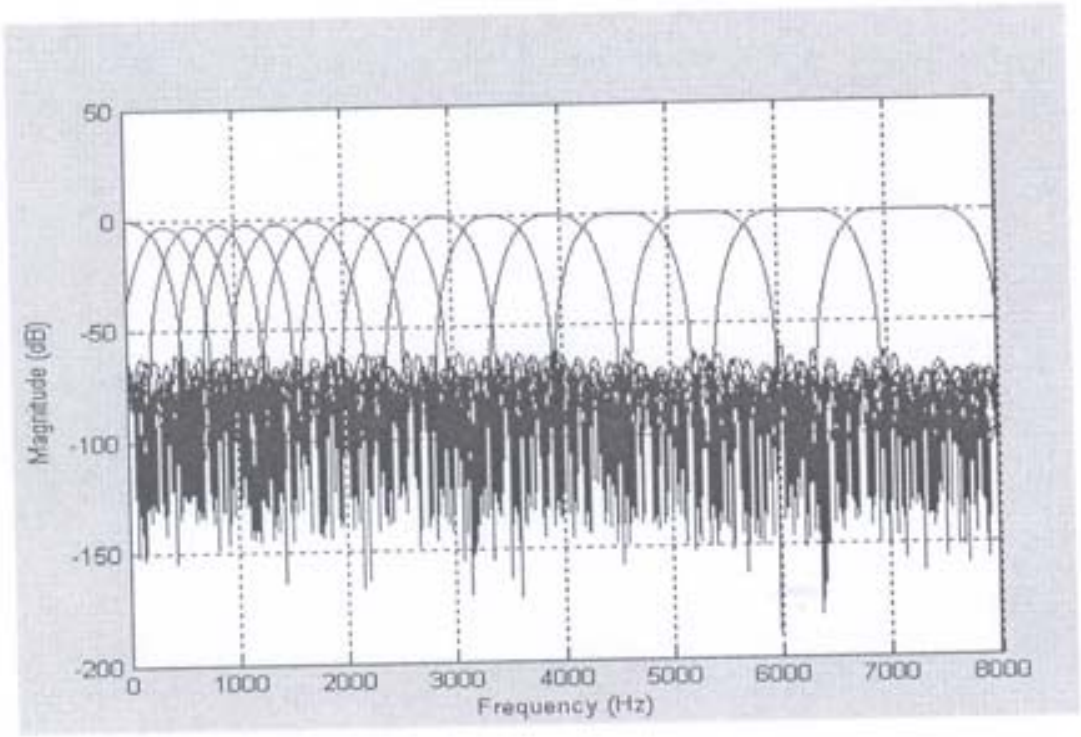

Figure 4: Frequency Responses of the 16 Frequency Bands of the Filter Bank

We further verify the magnitude response of our filter bank design after implementing the filter bank in circuit forms (for quantization considerations). The test procedure is as follows. First, we create a sound signal composed by frequency components ranging from 0 to 7.6 kHz. This sound signal is sampled with the sampling frequency of 16 kHz. The sampled data is quantized and converted to hexadecimal form before it is sent to the filter bank for processing. The output waveform (in hexadecimal format) is converted back to signal amplitude. The signal spectra of the output signals were plotted by using MATLAB Fast Fourier Transform (FFT). By comparing the input and output spectra, we could measure the attenuation provided by each bands of the filter bank. As a result, we conclude that our filter bank features at least >60 dB stopband attenuation and within ±1 dB.

In order to measure the amount of power reduction offered by our design, we perform power simulations on our design and a conventional filter bank [Mitra, 2001] which uses carry-save adders (CSA) for its multipliers [Parhami, 2000]. The simulations for both designs are performed on gate level (excluding the power dissipated by the RAM) in schematics. Table 3 shows the simulation result, which sees an improvement in power saving of as much as 50 percents. This result is somewhat optimistic, but useful for comparison purpose.

Table 3: Pre-layout Power Simulation Results of the Proposed and Conventional Design

	Conventional Design	Proposed Design
Power Dissipation (μW @ 1.1V, 1.024MHz)	270.8	134.7
Power Reduction	-50%	-

After the layout of the circuit is created, another power analysis simulation is performed to measure the power dissipated by the final circuit design. Based on post-layout simulation (physical layout), our final design dissipates only 248μW (excluding the RAM). This result is more accurate and is expected as the post-layout power simulation takes into the account of the parasitic by the RAM to be around 100μW @ 1.1V, 1.024 MHz, we are able to show that the total power dissipation of our filter bank design will be less than 400μW.

We have prototyped our filter bank design and sent for fabrication. Figure 5 shows the final layout of the filter bank. The dimension of the prototype IC is 3.2mm x 1.97mm, which is equivalent to a total area of ~6.3mm^2. For the core area only (excluding the I/O pads and RAM), our filter bank design occupies ~1.65mm^2. In summary, our proposed filter bank meets all our specifications and is suitable for a digital hearing aid application.

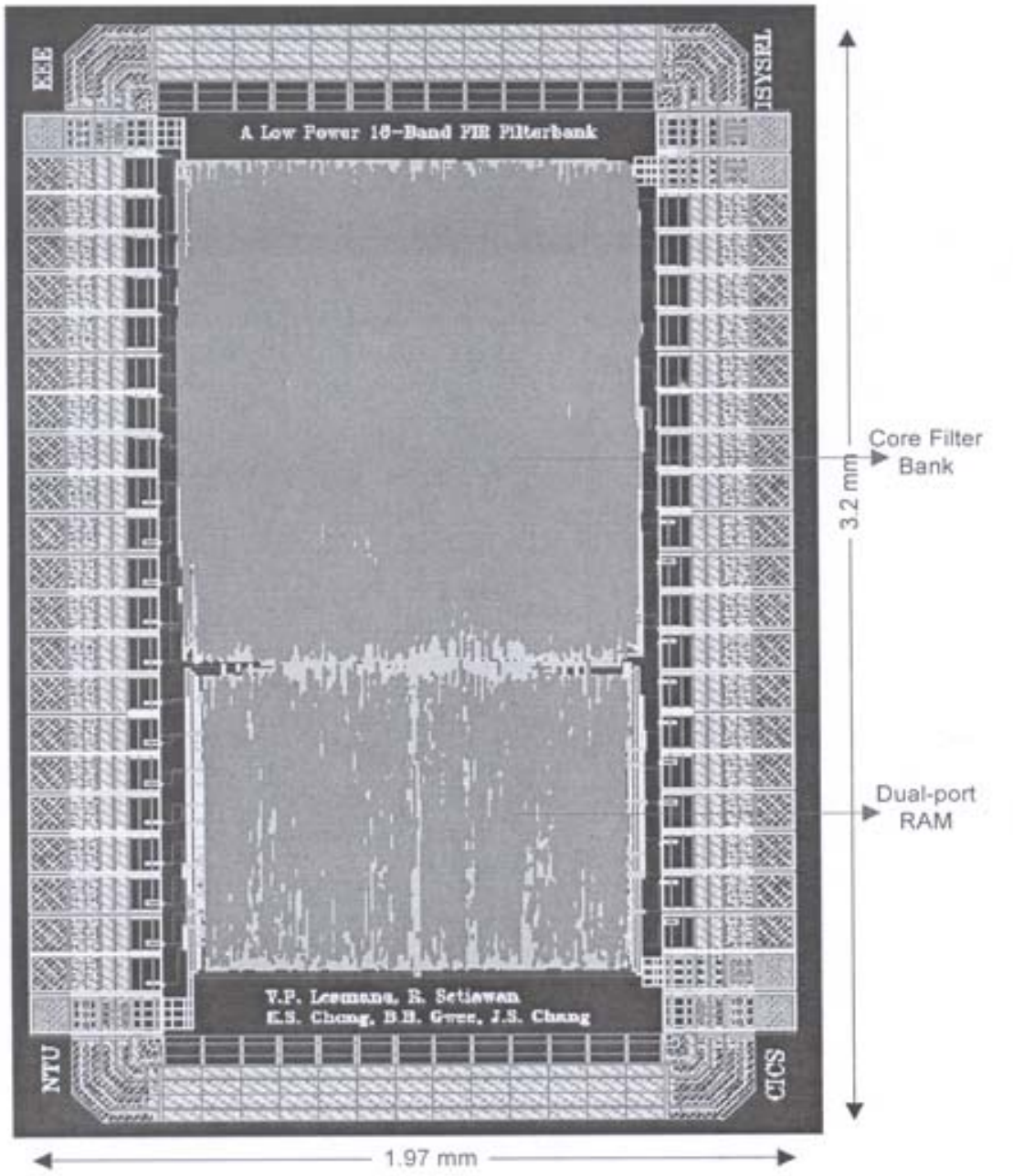

Figure 5: IC Layout for Fabrication

CONCLUSIONS

In this paper, we have proposed techniques to reduce power dissipation for a filter bank in digital hearing aid applications. The proposed algorithm is implemented for a 16-band critical bandwidth-like filter bank. The techniques reduce the amount of computations by optimizing the multiplication process.

The proposed filter bank features a minimum of 60 dB stopband attenuation, passband ripple less than ±1 dB and operates from 0 to 7.75 kHz frequency range with a sampling frequency of 16 kHz and clock frequency of 1.024 MHz. The overall filter bank response has a flat response when combined and the bandwidth of the filter bank has been carefully chosen to match human's hearing response; so the designed filter bank is suitable for digital hearing aid purposes.

The design is implemented using a commercial CMOS 0.35μm IC technology and a supply voltage of 1.1V. The design occupies an area of 6.3mm^2 (including the I/O pads and the dual port RAM). The core of the filter bank itself occupies only 1.65mm^2. The post-layout power simulation shows that the filter bank dissipates 250μW of power (not including the power dissipates by the RAM). When compared to the conventional approach (based on pre-layout simulation, it dissipates 50 percents lower power. The design has met all the project specification and the layout has been sent for fabrication.

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