A Low-voltage Micropower Asynchronous Multiplier for a Multiplierless FIR Filter

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ABSTRACT

We propose a low-voltage micropower (3.6μW @1.1V, 1MHz) 16×16-bit asynchronous signed multiplier based on a shift-add structure for an FIR filter for digital hearing instruments. We reduce the power and hardware in several ways. First, we use a sign-magnitude data representation and a maximum of 3 sum of Signed Power of Two terms for the multiplier operand. Second, we truncate the least significant partial products to yield a 16-bit signed product and propose an error correction means to reduce the quantization error. Third, we adopt a low power shifter design and employ our proposed latch adder. Finally, we propose a power efficient speculative delay line to enable the various circuit modules to operate asynchronously. We compare our design against reported designs, and show that our design exhibits the lowest power dissipation and requires a small IC area. We recommend our multiplier for low speed applications (<4MHz).

1. INTRODUCTION

The critical parameters of portable electronic devices with a mid-to-complex signal processing capability include low voltage (1.1V-1.4V) micropower (<1mA) operation and small IC area. Examples of such devices include the digital hearing instrument (hearing aid) and more recently, processors for wearable applications. These devices are usually powered by a small pill-size low voltage (1.1V-1.4V) low capacity (~100mAh) battery cell and the life-span of the cell is expected to exceed 100 hours. In view of the tight constraints placed on the remote power supply, the processor employed in these instruments is often clocked in the low MHz freq range, for example, 1-2MHz in digital hearing instruments. In these systems, the peripheral signal conditioning circuits are also often efficient, for example Class D amplifiers [1] are used in placed of more conventional linear amplifiers.

Design methodologies for low power low voltage designs [2] span from system level design to transistor-level design and the fabrication technology. At the system level, design considerations include the system architecture (e.g. minimum voltage operation (that limits the speed of the gates), type of signaling protocol (such as synchronous (sync) and asynchronous (async)), etc. The mid-level, on the other hand, include the architecture and design of the cells (in a cell library) such as the multiplier, etc.

The async approach (as opposed to the more common sync approach) is an emerging technology to reduce the power dissipation of digital circuits. The basic premise for this is that the signaling protocol between the different cells is localized, hence the elimination for the need of a complex global clock infrastructure. It is well established that in many sync microprocessors, the dynamic power dissipation of the complex clock infrastructure typically dissipates of the order of ~30% of the overall power. Furthermore, as the signaling in async designs is localized, async microprocessors have the potential to be faster than their sync counterparts. This is because the clock rate of the sync processors is timed to the slowest operation.

The multiplier is usually the most complex cell (and occupies the largest area) and often dissipates the highest power of all the cells in a cell library. In typical multipliers such as the Booth Array Multiplier, a large percentage (~30%) of the power dissipation is due to spurious switching [3,4] within the partial product generator and within the following complex adder stages. The usual design techniques to reduce the spurious switching include methods [5] that improve the synchronicity (timing) of the multiplier inputs, clock gating or latching intermediate signals, etc. If some degree of quantization error can be tolerated, the partial products can be truncated [5], e.g. in a 16x16 multiplication, the 32-bit partial product may be truncated to 18-bits and finally rounded to 16-bits. In this truncation, the amount of hardware is approximately halved, and the power dissipation similarly reduced.

A Multiplierless Multiplication (MM) approach may be employed for low power and small IC area considerations - the MM approach is an approach where there is no specific multiplication unit and multiplication is instead achieved by hardwired shifts and adders, and programmability is often restricted (see later). Several Finite-Impulse-Response (FIR) filters [6] employing this MM approach have been reported in literature. A programmable MM FIR filter was reported for high-speed application with a maximum of 3 canonical signed digits (CSD) [7]. However, as the CSD coefficients are not always with 3 non-zero digits, some power is unnecessarily dissipated to perform an addition with zero. A design [8] using programmable shifters and adders was reported but the power dissipation aspects were not considered. An async Break-point multiplier [9] for a hearing instrument with a maximum of three logic '1' bits in the magnitude of the Interpolated FIR filter coefficient (the multiplier operand) was reported. Although this design featured micropower and low circuit complexity, the limitation of three '1's makes the Break-point multiplier very restrictive (see later) and is practically useful only for very specific filter coefficients.

In this paper, we propose a 16×16-bit async signed multiplier with the MM approach and the design objectives are low voltage (1.1V) micropower (3.6μW @1MHz) operation and requiring a small IC area. To the best of our knowledge, this is the first

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single async MM multiplier that handles up to 3 Signed Power of Two (SPT) terms (as its multiplier operand) and utilizes a Signed Magnitude (SM) data representation (as opposed to 2's Complement). Its primary application is for an FIR filter for digital hearing instruments. The inputs to a multiplication process are the multiplicand and the multiplier operand. By being able to handle 3 SPT terms, our design is less restricted than reported designs [9] (in terms of the quantization error of the multiplier operand). We achieve micropower operation in several ways. First, by employing the SM data representation, there is less switching activities [2], hence reduced power dissipation. Second, we adopt a low power transmission gate shifter structure [10]. Third, we truncate the partial product terms to obtain a fixed word length of 16-bit signed product, thereby reducing the amount of hardware by approximately 50%. Fourth, we employ our novel Latch Adder (LA) [3] that features an adder with an integrated latch. Our LA dissipates less power than an independent adder and an independent latch, and occupies less IC area. We further employ a transparent latch (T-Latch) to block unnecessary switching. Finally, we propose a novel power efficient speculative delay line to time the multiplier asynchronously. We verify our proposed design by simulations and show the advantages of our design by comparing it against other sync and async multiplier designs. We also show that an FIR filter embodying our async MM multiplier yields a magnitude response suitable for many applications.

2. PROPOSED DESIGN

The equation of an FIR filter can be expressed as:

$$y(n) = \sum_{k=0}^{N} h(k)x(n-k) \qquad (1)$$

where $y(n)$ is the output, $x(n-k)$ are the inputs,
$h(k)$ are the filter coefficients, and
N is the order of the filter.

Eq. (1) shows that there are $N+1$ multiplications between the filter coefficients (multiplier operands) and the inputs (multiplicand operands). We adopt the MM approach by representing the multiplier operand as a minimum combination of several SPT terms and the multiplication process simply involves binary shift and add (or subtract) operations on multiplicand [11]. In this context, the multiplier operands are represented as:

$$h(k) = \sum_{m=1}^{L} b(m)2^{-f(m)} \qquad (2)$$

where $b(m) \in \{-1,1\}$, $h(k)$ is the k^{th} coefficient value, $f(m)$ is an integer, and L is the prescribed number of terms.

For example, for a coefficient = 0.46875, its representation in SPT terms (with binary signed digit representation) and in the more common 6-bit binary representation are shown in Eqs. (3) and (4) respectively:

$$0.46875 \approx 2^{-1}-2^{-5} = 0.1000\bar{1}\ ;\ \bar{1} \triangleq \text{subtraction} \qquad (3)$$

$$0.46875 \approx 2^{-2}+2^{-3}+2^{-4}+2^{-5} = 0.01111 \qquad (4)$$

It is well established that the representation as a sum of SPT terms has the advantage of reduced number of logic '1's. Our investigations have shown that the lesser number of '1's leads to lower power dissipation.

To simplify the hardware for an SM 16×16-bit signed multiplication, we modify the sum of the SPT representation with a sign bit:

$$h(k) = b(L)\times\left(2^{-f(L)} + \sum_{m=1}^{L-1}\frac{b(m)}{b(L)}2^{-f(m)}\right) \qquad (5)$$

where $b(L) = (-1)^{SG}$, $SG \in \{0,1\}$ as the sign bit; $2^{-f(L)}$ is the largest weight SPT term, L=3 in our proposed design, $h(k) \in (-1,1)$ for an FIR filter application.

The sign bit is essentially the sign of the largest weight SPT term and hence the sign of the multiplier operand. We remark that this sign bit modification for the SPT representation will lead to a design with reduced power dissipation.

3. HARDWARE IMPLEMENTATION

We depict the circuit block diagram of our proposed async MM multiplier with maximum of 3 SPT terms in Fig. 1. Since the 3 SPT terms require only 17 control signals, we store the multiplier operand as control words rather than actual 16-bit coefficients in memory. By doing this, we save on the additional decoding circuit hardware which would otherwise be required to convert the coefficient to control signals.

Our proposed design comprises 3 shift modules with T-Latch at the input, two latch adders/subtractors and an output multiplexer. Note that all the circuit modules handle 15-bit data while the sign bit is determined from a simple XOR gate. We employ the four-phase async handshaking protocol [9] with a novel speculative delay line to control the async MM multiplier asynchronously. Note that only modules that are necessary during the multiplication process are enabled and the remaining modules are disabled to block the unnecessary switching to save power.

The multiplicand operand is input to the 3 shift modules and each module handles 1 SPT term. The SPT terms are weighted more heavily from Shift Module 1 to Shift Module 3. We perform the addition or subtraction of two shifted multiplicands with an adder/subtractor, ADD/SUB.

We remark that because we know that Shift Module 1 always generates an output greater than Shift Modules 2 and 3, the subtraction can be performed without the need for magnitude comparison, and the circuit path remains simple. Put simply, no comparator is required for the SM subtraction and the probability of a high degree of switching in our design is low. Hence, we obtain low dynamic power dissipation. We will show that this is the case in Section 4 later.

We construct the shifter modules with a 4-level logarithmic structure transmission-gate multiplexer (with a low power stage arrangement [10]). We also employ T-Latches at the inputs of each shifter module to synchronize the multiplicand input, thereby reducing spurious switching. The shifters are also buffered to maintain a strong driving capability. We employ our LAs [3] (without the weak PMOS in Carry-Out) in the ADD/SUB modules and remark that by employing our LAs, the power dissipation is lower than a conventional design comprising a separate latch and a separate adder, and the IC area is also smaller. As the speed is not a critical parameter (<4MHz clock rate), we select the transistor aspect ratios (W/L) of our LAs to W/L=2 and this reduces the power dissipation due to smaller load capacitances.

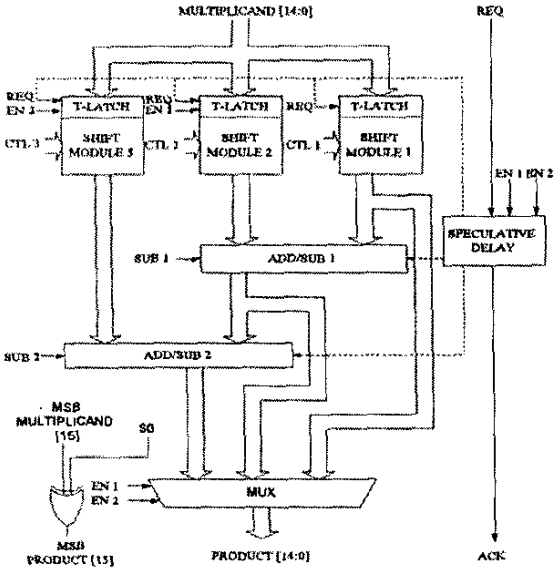

Fig. 1 Architecture of the proposed async MM multiplier

The LAs are timed and enabled after a certain delay determined from the delay line. This is to reduce spurious switching due to the poorly synchronized outputs from the different shift modules to the ADD/SUB modules.

We propose a power efficient speculative delay line to realize this delay line and show its block circuit diagram in Fig. 2. We design a single worst-case delay that is partitioned into three completion delays and are to be enabled chronologically. Furthermore, as we store enable control signals, *EN*1 and *EN*2 (as part of the 17 control signals), in the control words, we do not require any additional abortion circuits [12] to select the respective completion signal. Our design is novel because we include AND gates that enable the ADD/SUB modules that contribute as part of the delay while simultaneously serving as blocking gates. This is so that the request signal *REQ* does not toggle the entire delay line in all occasions. In addition, both ADD/SUB modules share a single worst-case adder delay (ADDER DELAY 2). Our objective here is to reduce the power dissipation (due to reduced spurious switching in the delay line) and to speed up the MM process. For example, in a single shift operation, the ADDER DELAY 1 and ADDER DELAY 2 are disabled. When the *REQ* is asserted, only the SHIFT DELAY portion toggles and generates the acknowledge signal, *ACK*, after the shifter delay.

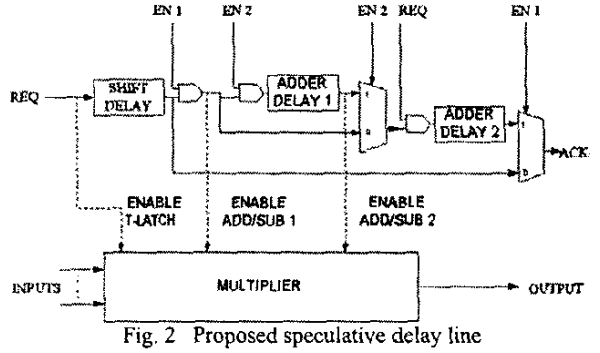

Fig. 2 Proposed speculative delay line

We remark that as the operation in ADD/SUB 1 is usually completed earlier than the worst-case delay, we design ADDER DELAY 1 in Fig. 2 to be faster than ADDER DELAY 2. This allows ADD/SUB 2 to operate earlier, thereby reducing the total worst-case delay. In summary, our proposed speculative delay line improves the performance of our async MM multiplier and is more power efficient (over reported delay lines).

4. SIMULATION RESULTS

We verify our proposed async MM multiplier by means of HSPICE computer simulations @ 1.1V, 1 MHz (the input vectors also change at this rate, and with device fabrication parameters based on a 0.3μm CMOS process). To fairly compare our proposed async MM multiplier design against reported designs, in particular [5, 9, and 13; refer to Table 1], we also re-implement and simulate these reported designs with the same abovementioned conditions. We obtain the power dissipation for the different designs using NANOSIM.

We apply 500 sets of random multiplicand and multiplier operands to the different multiplier designs. The random multiplier operands have a maximum of 3 '1's, to accommodate the very restricted data representation of the Break-point multiplier; we reiterate that our async MM multiplier design with a maximum of 3 SPT terms is much more general than that of the Break-point multiplier. Note that the multiplicand operands applied to the proposed design are represented in SM while their equivalent is represented in 2's complement for the other multipliers. To emulate the conditions of a typical FIR filter, the ratio of 3, 2 and 1 SPT terms is 63%, 12% and 25% respectively.

We summarize in Table 1 a comparison of the different multipliers. In general, the number of transistors is indicative of the IC area and a small IC area is desired.

Table 1 Power, average switching, number of transistors, average delay and PDP at V_{DD}=1.1V@1MHz

16×16-bit Multiplier Design	Power (μw)	Avg Switch-ing	No. of Transis-tors	Avg Delay (ns)	PDP (pJ)
Sync [13]	9.16	742	9204	82*	0.75
Sync trunc [5]	5.85	479	4964	59*	0.35
Async Bk-pnt [9]	5.22	468	2260	84	0.44
Our Async design	3.58	329	2898	116	0.42

* Worst case delay for synchronous clock system

From Table 1, we make the following remarks:

(i) The proposed async MM multiplier features the lowest power dissipation of all designs and this is reflected in its smallest number of transistor switchings. The Sync multiplier, as expected, dissipates the highest power because it is a full untruncated 16x16-bit multiplier. Although the proposed design has a lower power (~39%) than the sync truncated multiplier due to its simpler structure and reduced spurious switching, the sync truncated multiplier is more general (with a full 16-bit multiplier operand data representation). The proposed design also dissipates lower power (~31%) than the reported Break-point multiplier because of the implementation of our LAs and the

power efficient shifter structure. We reiterate that in addition to this power advantage, the proposed design is far more general (less quantization error) than the Break-point multiplier.

(ii) The proposed async MM multilplier requires a small number of transistors. This translates to the relatively small IC area (~28% more than the Async Break-point multiplier, but ~69% and ~42% less than the Sync multiplier and Sync truncated multiplier respectively).

(iii) The proposed async MM multiplier has the longest delay of all the multipliers. The average delay is 116ns and a cycle delay is 175ns (including average reset delay) and this translates to a 5.7MHz operation. We reiterate that the objective of our design is not for high speed but instead for applications where the clock is <4MHz, for example in a digital hearing instrument where the clock rate is typically between 1-2MHz. Although not shown in Table 1, the worst-case delay is 219ns (including reset delay), or equivalently, 4.6MHz. In this worst-case, the speed is still sufficient for many applications.

In Table 2, we show the effectiveness of the proposed speculative delay line that reduces the average delay depending on the distribution of the number SPT terms – the speed of the multiplication process increases with a smaller number of SPT terms. We remark that the delay of sync multipliers remains constant independent of the number of SPT and this is attributed to the limitation of the critical path.

Table 2 A Comparison of the average delay for various number of SPT terms

16×16-bit Multiplier Design	Average delay (ns)		
	Case 1*	Case 2*	Case 3*
Sync [13]	82#	82#	82#
Sync truncated [5]	59#	59#	59#
Aync Bk-pnt [9]	84	81	69
Our Async design	116	104	75

*Case 1: 3 SPT(63%), 2 SPT (12%), 1 SPT (25%)
Case 2: 3 SPT (25%), 2 SPT (50%), 1 SPT (25%)
Case 3: 3 SPT (25.6%), 2 SPT (17.6%), 1 SPT (56.8%)
Worst case delay for synchronous clock system

We have shown thus far, the attractive power dissipation attribute of the proposed async MM multiplier. We will now demonstrate the application of the proposed async MM multiplier for a practical 76 tap FIR lowpass filters with 400Hz pass-band and –43dB stop-band attenuation. We depict in Fig. 3 the simulated frequency response of the filter using MATLAB, and remark that the response of the FIR filter embodying our async MM multiplier obtained a stop-band attenuation of -40dB. We note that there is some discrepancy in the stop-band and this is attributed to the truncation of the multiplier. However, this discrepancy is not usually a problem in many applications as the attenuation is already high in the stop-band.

We finally remark that we reduce the quantization error from the truncation by adding a correction to the least significant bit (LSB) of the proposed async MM multiplier. We do this by connecting the carry-in of the ADD/SUB 1 to V_{DD}, thereby limiting the maximum error to ≤ 2 LSBs.

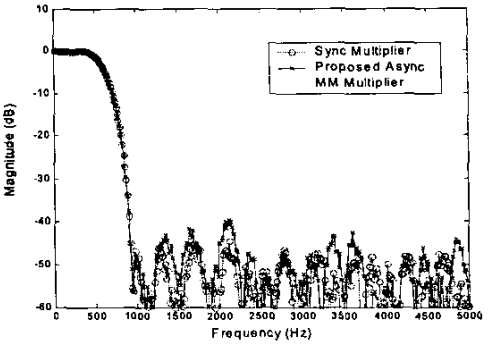

Fig. 3 Frequency response of a low pass FIR filter based on the standard and proposed async MM multipliers

5. CONCLUSIONS

We have proposed and designed a low-voltage micropower 16×16-bit async signed truncated multiplier with multiplierless multiplication approach based on the shift-add structure. To reduce the power dissipation, we have employed the sign magnitude data and the sum of SPT terms representation, truncated the partial product hardware by half, employed the low power shifter and our LA, and proposed a novel speculative delay line. We have shown that our proposed design exhibits a lowest power dissipation compared to reported designs. In summary, our proposed 16×16-bit async signed multiplier is appropriate for low voltage micropower multiplierless FIR filters for a digital hearing instrument.

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