Juha Yli-Kaakinen — List of Publications

Ten most important publications are marked with asterix (★)

1 Journal Publications

[J1] ★ J. Yli-Kaakinen and T. Saramäki, "Design of low-sensitivity and low-noise recursive digital filters using a cascade of low-order lattice wave digital filters," *IEEE Trans. Circuits Syst. II*, vol. 46, pp. 906–914, July 1999. DOI: 10.1109/82.775386. (26 citing documents: [296, 117, 179, 195, 25, 159, 24, 18, 145, 28, 170, 127, 16, 181, 281, 27, 23, 169, 230, 189, 89, 221, 180, 241, 29, 26]).

[J2] ★ J. Yli-Kaakinen, T. Kupiainen, M. Hu, R. Uusikartano, and M. Renfors, "Multirate digital filter design for a PAL TV modulator," *IEEE Trans. Consumer Electron.*, vol. 45, no. 3, pp. 970–974, Aug. 1999. DOI: 10.1109/82.775386. (3 citing documents: [297, 255, 86])

[J3] ★ T. Saramäki, J. Yli-Kaakinen, and H. Johansson, "Optimization of frequency-response-masking based FIR filters," *J. Circuits, Syst., Computers*, vol. 12, no. 5, pp. 563–591, Oct. 2003.[1] DOI: 10.1142/S0218126603001070. (24 citing documents: [150, 277, 148, 152, 283, 275, 62, 113, 149, 151, 153, 276, 156, 15, 167, 157, 132, 79, 280, 250, 147, 220, 219, 115]).

[J4] ★ J. Yli-Kaakinen and T. Saramäki, "Multiplication-free polynomial-based FIR filters with an adjustable fractional delay," *Circuits, Systems, and Signal Processing*, Special Issue on Computationally Efficient Digital Filters: Design Techniques and Applications, vol. 25, no. 2, pp. 265–294, 2006. DOI: 10.1007/s00034-005-2507-3. (27 citing documents: [109, 100, 17, 280, 1, 240, 198, 216, 110, 239, 245, 215, 67, 71, 37, 285, 111, 243, 116, 72, 22, 2, 58, 114, 21, 267, 242]).

[J5] ★ J. Yli-Kaakinen and T. Saramäki, "A systematic algorithm for the design of lattice wave digital filters with short coefficient wordlength," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 8, pp. 1838–1851, Aug. 2007. DOI: 10.1109/TCSI.2007.902513. (20 citing documents: [30, 26, 212, 236, 92, 186, 184, 237, 211, 95, 70, 73, 214, 182, 213, 2, 119, 187, 209, 233]).

[J6] ★ J. Yli-Kaakinen and T. Saramäki, "An efficient algorithm for the optimization of FIR filters synthesized using the multistage frequency-response masking approach," *Circuits, Systems, Signal Processing*, vol. 30, no. 1, pp. 157–183, 2011. DOI: 10.1007/s00034-010-9216-2. (12 citing documents: [225, 224, 226, 20, 194, 137, 88, 112, 254, 252, 66, 249]).

[J7] ★ M. Renfors, J. Yli-Kaakinen, and f. harris, "Analysis and design of efficient and flexible fast-convolution based multirate filter banks," *IEEE Trans. Signal Processing*, vol. 62, no. 15, pp. 3768–3783, Aug. 2014. DOI: 10.1109/TSP.2014.2330331. (2 citing documents: [208, 78]).

[J8] J. Yli-Kaakinen, V. Lehtinen, and M. Renfors, "Multirate charge-domain filter design for RF-sampling multi-standard receiver," to appear in *IEEE Trans. Signal Processing*, 10 pages. DOI: 10.1109/TCSI.2014.2363514.

[J9] J. Yli-Kaakinen and M. Renfors, "Optimization of flexible filter banks based on fast-convolution," submitted to *The Journal of Signal Processing Systems*, 8 pages.

[J10] M. Renfors, J. Yli-Kaakinen, F. Bader, A. Amri, Y. Medjahdi, D. Roviras, D. le Ruyet, H. Shaiek, B. Chaitanya, L. Martinod, and P, Mége "Flexible multi-carrier structure enabling migration to future generation broadband professional communication services," submitted to *IEEE Trans. Commun.*, 10 pages.

2 Conference Publications

[C1] J. Yli-Kaakinen and T. Saramäki, "Design of very low-sensitivity and low-noise recursive digital filters using a cascade of low-order wave lattice filters," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. V, Monterey, CA, USA, May 31–June 3 1998, pp. 404–408.[2] DOI: 10.1109/ISCAS.1998.694513.

[1] Selected to be a best paper for the Special Issue entitled *Frequency-Response Masking Technique* of the *Journal of Circuits, Systems, and Computers.*

[2] Selected to the Special Issue entitled *1998 International Symposium on Circuits and Systems* of the *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*.

[C2] J. Yli-Kaakinen and T. Saramäki, "An efficient algorithm for the design of lattice wave digital filters with short coefficient wordlength," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. III, Orlando, FL, USA, May 30–June 2 1999, pp. 443–448. DOI: 10.1109/ISCAS.1999.778880. (15 citing documents: [36, 206, 205, 34, 40, 272, 204, 273, 238, 207, 33, 35, 256, 257, 3]).

[C3] J. Yli-Kaakinen, M. Hu, R. Uusikartano, T. Kupiainen, and M. Renfors, "Digital filter design for a PAL TV modulator," in *Proc. IEEE Int. Conf. Consumer Electronics (ICCE)*, Los Angeles, CA, USA, June 22–24 1999, pp. 260–261.[3] DOI: 10.1109/ICCE.1999.785257.

[C4] J. Yli-Kaakinen, M. Hu, T. Kupiainen, and M. Renfors, "Digital filter design for a PAL TV modulator," in *Proc. IEEE Int. Conf. Electr. Circuits Syst. (ICECS)*, Pafos, Cyprus, Sep. 5–8 1999, pp. 249–252. DOI: 10.1109/ICECS.1999.812270.

[C5] M. Hu, J. Yli-Kaakinen, M. Renfors, and O. Vainio, "A multiplier-free design for an integrated digital VSB filter using wave digital all-pass sections," in *Proc. 8th IEEE Int. Symp. on Integrated Circuits, Devices and Systems (ISIC)*, Singapore, Sept. 8–10 1999, pp. 126–129.

[C6] J. Yli-Kaakinen and T. Saramäki, "An algorithm for the design of multiplierless approximately linear-phase lattice wave digital filters," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. 2, Geneva, Switzerland, May 28–31 2000, pp. 77–80. DOI: 10.1109/ISCAS.2000.856262. (20 citing documents: [165, 163, 145, 106, 105, 162, 85, 103, 160, 189, 204, 164, 207, 139, 161, 104, 166, 107, 108, 187])

[C7] T. Saramäki and J. Yli-Kaakinen, "Design of digital filters and filter banks by optimization: Applications," in *Proc. X European Signal Processing Conf. (EUSIPCO)*, Tampere, Finland, Sept. 5–8 2000, also reprinted in *Proc. IEEE 1st South American Workshop on Circuits Syst. (SAWCAS)*, Rio de Janeiro, Brazil, Nov. 20–22 2000. (16 citing documents: [90, 75, 93, 217, 56, 74, 281, 94, 91, 259, 84, 20, 235, 234, 69])

[C8] J. Yli-Kaakinen and T. Saramäki, "An algorithm for the optimization of pipelined recursive digital filters," in *Proc. Euro. Conf. Circuit Theory Design (ECCTD)*, vol. 2, Helsinki, Finland, Aug. 2001, pp. 225–228.

[C9] ★ J. Yli-Kaakinen and T. Saramäki, "A systematic algorithm for the design of multiplierless FIR filters," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. II, Sydney, Australia, May 6–9 2001, pp. 185–188. DOI: 10.1109/ISCAS.2001.921038. (72 citing documents: [143, 81, 144, 55, 270, 14, 271, 126, 189, 10, 222, 176, 192, 193, 288, 123, 161, 260, 172, 291, 104, 294, 290, 175, 289, 287, 166, 293, 261, 286, 9, 11, 292, 246, 173, 174, 282, 125, 124, 98, 278, 138, 229, 228, 19, 253, 266, 118, 73, 223, 46, 135, 268, 87, 49, 41, 45, 7, 269, 131, 43, 264, 50, 48, 47, 42, 233, 265, 267, 8, 51, 44])

[C10] T. Saramäki and J. Yli-Kaakinen, "Optimization of frequency-response-masking based FIR filters with reduced complexity," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Scottsdale, AZ, USA, May 26–29 2002, pp. 225–228. DOI: 10.1109/ISCAS.2002.1010201. (12 citing documents: [154, 146, 53, 263, 283, 277, 275, 141, 142, 128, 129, 276])

[C11] J. Yli-Kaakinen and T. Saramäki, "Multiplier-free polynomial-based FIR filters with an adjustable fractional delay," in *Proc. IEEE Int. Conf. Electr. Circuits Syst. (ICECS)*, vol. III, Dubrovnik, Croatia, Sept. 15–18 2002, pp. 1167–1170. DOI: 10.1109/ICECS.2002.1046460. (4 citing documents: [189, 171, 59, 116])

[C12] T. Saramäki and J. Yli-Kaakinen, "A systematic technique for designing multiplierless lattice wave digital filters and FIR filters," in *Proc. 6th Int. Conf. Digital Signal Process. and its Applications, (DSPA)*, vol. 6, no. 1, Moscow, Russia, Mar. 31–Apr. 2 2004, pp. 104–105.

[C13] J. Yli-Kaakinen and T. Saramäki, "A systematic algorithm for the design of multiplierless lattice wave digital filters," in *Proc. 2004 IEEE Int. Symp. Control., Commun., Signal Process. (ISCCSP)*, Hammamet, Tunisia, Mar. 21–24 2004, pp. 415–418. DOI: 10.1109/ISCCSP.2004.1296311. (2 citing document: [189, 89])

[C14] J. Yli-Kaakinen, T. Saramäki, and R. Bregović, "An algorithm for the design of multiplierless two-channel perfect reconstruction orthogonal filter banks," in *Proc. 2004 IEEE Int. Symp. Control., Commun., Signal Process. (ISCCSP)*, Hammamet, Tunisia, Mar. 21–24 2004, pp. 393–396. DOI: 10.1109/ISCCSP.2004.1296317. (10 citing documents: [189, 279, 200, 191, 188, 185, 183, 190, 46, 48])

[C15] J. Yli-Kaakinen, T. Saramäki, and Y. J. Yu, "An efficient algorithm for the optimization of FIR filters synthesized using the multi-stage frequency-response masking approach," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. V, Vancouver, Canada, May 23–26 2004, pp. 540–543. DOI: 10.1109/ISCAS.2004.1329709. (8 citing documents: [128, 99, 276, 301, 168, 130, 274])

[3] Selected to the Special Issue entitled *1999 International Conference on Consumer Electronics* of the *IEEE Transactions on Consumer Electronics*.

[C16] J. Yli-Kaakinen and T. Saramäki, "An algorithm for the optimization of adjustable fractional-delay all-pass filters," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. III, Vancouver, Canada, May 23–26 2004, pp. 153–156. DOI: 10.1109/ISCAS.2004.1328706. (29 citing documents: [64, 65, 299, 6, 196, 102, 5, 17, 140, 248, 101, 4, 231, 300, 155, 232, 60, 247, 199, 197, 39, 52, 239, 202, 57, 201, 203, 274, 298])

[C17] J. Yli-Kaakinen and T. Saramäki, "Design and implementation of multiplierless adjustable fractional-delay all-pass filters," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Kobe, Japan, May 23–26 2005, pp. 1827–1830. DOI: 10.1109/ISCAS.2005.1464965. (2 citing documents: [63, 119])

[C18] J. Yli-Kaakinen and T. Saramäki, "A systematic algorithm for designing multiplierless computationally efficient recursive decimators and interpolators," in *Proc. 2005 IEEE Int. Symp. Image and Signal Process. Analysis (ISPA)*, Zagreb, Croatia, Sept. 15–17 2005, pp. 167–172. DOI: 10.1109/ISPA.2005.195404. (1 citing document: [209])

[C19] J. Yli-Kaakinen and T. Saramäki, "Approximately linear-phase recursive digital filters with variable magnitude characteristics," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Island of Kos, Greece, May 21–24, 2006, pp. 5227–5230. DOI: 10.1109/ISCAS.2006.1693811. (4 citing documents: [125, 124, 12, 136])

[C20] T. Saramäki and J. Yli-Kaakinen, "A novel systematic approach for synthesizing multiplication-free highly-selective FIR half-band decimators and interpolators," in *Proc. IEEE Acia Pacific Conf. Circuits Syst. (APCCAS)*, Singapore, Dec. 4–7 2006, pp. 920–923. DOI: 10.1109/APCCAS.2006.342211. (9 citing documents: [68, 13, 79, 77, 80, 295, 76, 82, 83])

[C21] V. I. Anzova, J. Yli-Kaakinen, and T. Saramäki, "An algorithm for the design of multiplierless IIR filters as a parallel connection of two all-pass filters," in *Proc. IEEE Acia Pacific Conf. Circuits Syst. (APCCAS)*, Singapore, Dec. 4–7 2006, pp. 744–747. DOI: 10.1109/APCCAS.2006.342115. (7 citing documents: [241, 251, 240, 227, 119, 252, 209])

[C22] J. Yli-Kaakinen and T. Saramäki, "Efficient recursive digital filters with variable magnitude characteristics," in *Proc. Nordic Signal Processing Symposium (NORSIG)*, Reykjavík, Iceland, June 7–9 2006, pp. 30–33. DOI: 10.1109/NORSIG.2006.275268.

[C23] J. Yli-Kaakinen and T. Saramäki, "An efficient structure for FIR filters with an adjustable fractional delay," in *Proc. Digital Signal Processing and its Applications (DSPA)*, Moscow, Russia, Mar. 29–31 2006, vol. 2, pp. 617–623. (6 citing documents: [125, 124, 215, 67, 37, 114])

[C24] ★ J. Yli-Kaakinen and T. Saramäki, "A simplified structure for FIR filters with an adjustable fractional delay," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, New Orleans, LA, USA, May. 27–30 2007, pp. 3439–3442. DOI: 10.1109/ISCAS.2007.378366. (11 citing documents: [17, 244, 215, 67, 37, 258, 243, 72, 115, 284, 262])

[C25] V. I. Anzova, J. Yli-Kaakinen and T. Saramäki, "A genetic-based algorithm for the design of multiplierless halfband IIR filters," in *Proc. 44th Int. Scientific Conf., Inform., Commun. Energy Syst. Technol. (ICEST)*, Veliko Tarnovo, Bulgaria, June 25–27 2009, pp. 227–230. (2 citing documents: [178, 210])

[C26] T. Saramäki and J. Yli-Kaakinen, "An improved approach for the synthesis of multiplication-free highly-selective FIR half-band decimators and interpolators," (invited paper) in *Proc. 12th Int. Symp. Integr. Circuits (ISIC)*, Singapore, Dec. 14–16 2009, pp. 344–351.

[C27] J. Yli-Kaakinen and M. Renfors, "Fast-convolution filter bank approach for non-contiguous spectrum use," in *Proc. Future Network and MobileSummi*, Lisbon, Portugal, July 3–5 2013. (7 citing documents: [121, 122, 38, 96, 133, 120, 134])

[C28] M. Renfors and J. Yli-Kaakinen "Timing offset compensation in fast-convolution filter bank based waveform processing," in *Proc. Int. Symp. Wireless Communication Systems*, Ilmenau, Germany, Aug. 27–30 2013. (2 citing documents: [177, 133])

[C29] J. Yli-Kaakinen and M. Renfors, "Optimization of flexible filter banks based on fast-convolution," in *Proc. Int. Conf. Acoustics, Speech, and Signal Processing*, Florence, Italy, May 4–9 2014, pp. 8342–8345. DOI: 10.1109/ICASSP.2014.6855223. (1 citing document: [61])

[C30] M. Renfors and J. Yli-Kaakinen, "Channel equalization in fast-convolution filter bank based receivers for professional mobile radio," in *Proc. European Wireless 2014*, Barcelona, Spain, May 14–16 2014, pp. 844–848.

[C31] J. Yli-Kaakinen and M. Renfors, "Multi-mode filter bank solution for broadband PMR coexistence with TETRA," in *Proc. European Conference on Networks and Communications*, Bologna, Italy, June 23–24 2014. DOI: 10.1109/EuCNC.2014.6882664.

[C32] M. Renfors and J. Yli-Kaakinen, “Flexible fast-convolution implementation of single-carrier waveform processing,” submitted to *Int. Conf. on Communications*, London, UK, June 8–12 2015.

[C33] Kai Shao, J. Alhava, J. Yli-Kaakinen, and M. Renfors “Fast-convolution implementation of filter bank multicarrier waveform processing,” to appear in *Proc. Int. Symp. on Circuits and Systems*, Lisbon, Portugal, May 24–27 2015.

3 Book Chapters

[B1] ★ J. Yli-Kaakinen and T. Saramäki, “A systematic algorithm for the synthesis of multiplierless lattice wave digital filters,” invited book chapter in *Digital Filters*, F. P. G. Márquez (Ed.), Intech, Apr. 2011, ch. 11, pp. 257–289.

4 Theses

[T1] J. Yli-Kaakinen, *Optimization of Recursive Digital Filters for Practical Implementation*, Dipl. Eng. Thesis, Dept. of Elect. Eng., Tampere University of Technology, Finland, June 1998. (Citing document: [296])

[T2] J. Yli-Kaakinen, *Optimization of Digital Filters for Practical Implementations*, Dr. Tech. Thesis, Dept. of Inform. Tech., Tampere University of Technology, Finland, May 2002. (6 citing documents: [218, 32, 158, 31, 97, 54])

5 Other Scientific Publications

[O1] T. Saramäki and J. Yli-Kaakinen, “Design of digital filters and filter banks by optimization: Applications,” Tampere International Center for Signal Processing, Tech. Rep. No. 15, Apr. 2002, 119 pages.

[O2] M. Renfors, J. Yli-Kaakinen, A. Lolou, X. Mestre, S. Nedić, S. Jošilo, M. Pejović, L. Martinod, and D Rakić, “FB-MC and enhanced OFDM schemes,” ICT-EMPhAtiC (Enhanced Multicarrier Techniques for Professional Ad-Hoc and Cell-Based Communications) Deliverable D2.1, Oct. 2013.

[O3] D. Rakić, L. Martinod, Y. Medjahdi, D. le Ruyet, F. Bader, 1D. Petrov, S. Nedić, and J. Yli-Kaakinen , “Multimode, non-uniform filterbank,” ICT-EMPhAtiC (Enhanced Multicarrier Techniques for Professional Ad-Hoc and Cell-Based Communications) Deliverable D2.2, Mar. 2014.

[O4] E. Kofidis, A. Beikos, M. Renfors, J. Yli-Kaakinen, L. G. Baltar, L. Martinod, P. Mé, L. Féty, and D. Le Ruyet, “Training Design and Algorithms for channel estimation,” ICT-EMPhAtiC (Enhanced Multicarrier Techniques for Professional Ad-Hoc and Cell-Based Communications) Deliverable D3.1, Mar. 2014.

[O5] S. Nedić, S. Jošilo, V. Stanivuk, M. Narandžić, M. Renfors, J. Yli-Kaakinen, E. Kofidis, A. Beikos, and R. Zakaria, “Adaptive equalization and successive self-interference cancellation (SIC) methods,” ICT-EMPhAtiC (Enhanced Multicarrier Techniques for Professional Ad-Hoc and Cell-Based Communications) Deliverable D3.2, Apr. 2014.

[O6] C. Mavrokefalidis, E. Kofidis, A. Rontogiannis, A. Beikos, M. Renfors, J. Yli-Kaakinen, and J. Louveaux “MIMO channel estimation and data detection,” ICT-EMPhAtiC (Enhanced Multicarrier Techniques for Professional Ad-Hoc and Cell-Based Communications) Deliverable D4.2, Mar. 2014.

[O7] D. Gregoratti, X. Mestre, M. Renfors, J. Yli-Kaakinen, N. Passas, D. Tsolkas, V. Ringset, S. Nedić, M. Narandžic, Stefan Tomić, L. Marijanović “Application of the nonuniform filterbank for spectrum sensing in a cognitive radio,” ICT-EMPhAtiC (Enhanced Multicarrier Techniques for Professional Ad-Hoc and Cell-Based Communications) Deliverable D8.1, May 2014.

Citing Documents (359 Citations in 301 documents)

[1] M. Abbas, O. Gustafsson, and H. Johansson, “Scaling of fractional delay filters based on the Farrow structure,” in *Proc. IEEE Int. Symp. Circuits Syst.*, Taipei, Taiwan, May 24–27, 2009, pp. 489–492. DOI: 10.1109/ISCAS.2009.5117792.

[2] —, “On the fixed-point implementation of fractional-delay filters based on the farrow structure,” *IEEE Trans. Circuits Syst. I*, vol. 60, no. 4, pp. 926–937, Apr. 2013. DOI: 10.1109/TCSI.2013.2244272.

[3] J. M. Abdul-Jabbar, “A simple analytic design procedure for lattice wave digital filters with approximate linear phase,” *Basrah Journal for Engineering Science*, 2011. [Online]. Available: http://www.uobasrah.edu.iq/images/journal/11.pdf.

[4] S. U. Ahmad, “Design of digital filters using genetic algorithms,” PhD thesis, Dept. of Electrical and Computer Eng., Univ. of Victoria, Canada, 2008. [Online]. Available: http://hdl.handle.net/1828/1294.

[5] S. U. Ahmad and A. Antoniou, “A genetic algorithm for the design of tunable fractional-delay allpass IIR filter structures,” in *Canadian Conf. Electr. Comput. Eng.*, Vancouver, BC, Canada, 2007, pp. 733–736. DOI: 10.1109/CCECE.2007.188.

[6] —, “Design of digital filters using genetic algorithms,” in *6th IEEE Int. Symp. Signal Process. Information Technol.*, Vancouver, Canada, 2006. DOI: 10.1109/CCECE.2007.188.

[7] L. Aksoy, P. Flores, and J. Monteiro, "SIREN: A depth-first search algorithm for the filter design optimization problem," in *23rd ACM Int. Conf. Great Lakes Symposium on VLSI (GLSVLSI 2013)*, Paris, France, 2013, pp. 179–184. DOI: 10.1145/2483028.2483087.

[8] —, "SIREN: A depth-first search algorithm for the filter design optimization problem," in *23rd ACM Int. Conf. Great Lakes Symposium on VLSI (GLSVLSI 2013)*, Paris, France, 2013, pp. 179–184. DOI: 10.1145/2483028.2483087.

[9] M. Aktan, "High-level power efficient synthesis of FIR based digital systems," PhD thesis, Boğfaziçi University, Istanbul, Turkey, 2007. [Online]. Available: http://www.belgeler.com/blg/kcp/high-level-power-efficient-synthesis-of-fir-based-digital-systems-sonlu-durtu-yanitli-suzgec-temelli-sayisal-sistemlerin-yuksek-seviyede-guc-verimliligine-gore-sentezi.

[10] M. Aktan and G. Dündar, "Design of digital filters for low power applications using integer quadratic programming," in *Integrated Circuit and System Design*, vol. 3728/2005, ser. Lecture Notes in Computer Science, Springer Berlin / Heidelberg, 2005, pp. 137–145. DOI: 10.1007/11556930_15.

[11] M. Aktan, A. Yurdakul, and G. Dündar, "An algorithm for the design of low-power hardware-efficient FIR filters," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 6, pp. 1536–1545, Jul. 2008. DOI: 10.1109/TCSI.2008.917997.

[12] A. Alimohammad and S. F. Fard, "FPGA implementation of isotropic and nonisotropic fading channels," *IEEE Trans. Circuits Syst. I*, vol. 60, no. 11, pp. 796–800, 2013. DOI: 10.1109/TCSII.2013.2281768.

[13] A. Amirhossein, "Signal filtering and filter design techniques," pat. WO2008097595, Aug. 2008. [Online]. Available: http://www.wipo.int/patentscope/search/en/WO2008097595.

[14] V. Anzova, K. Ivanova, and G. K. Stoyanov, "Design of multiplierless linear phase FIR filters with minimum number of power-of-two-terms-coefficients," in *Proc. Electronics'2004*, Sozopol, Bulgaria, Sep. 22–22, 2004, pp. 168–173. [Online]. Available: http://ecad.tu-sofia.bg/et/2004/Papers/Circuits%20and%20Systems/Paper-V_Anzova.pdf.

[15] P. Arian, "Computationally efficient decimators, interpolators, and narrow transition-band linear-phase finite impulse response (FIR) filters," Dr. Tech. dissertation, Dept. of Inform. Tech., Tampere Univ. of Tech, Finland, Tampere, Finland, Feb. 2007. [Online]. Available: http://dspace.cc.tut.fi/dpub/bitstream/handle/123456789/69/arian.pdf?sequence=1.

[16] P. Åström, "Custom datapaths for DSP ASICs: Methodology and implementation," No. 36, PhD thesis, Dept. of Electroscience, Lund University, Sweden, May 2003. [Online]. Available: http://theses.lub.lu.se/postgrad/search.tkl?field_query1=pubid&query1=tec_654&recordformat=display.

[17] J.-F. Bercher and C. Berland, "Envelope and phase delays correction in an EER radio architecture," *Analog Integr. Circ. Signal Process.*, vol. 55, no. 1, pp. 21–35, Apr. 2008. DOI: 10.1007/s10470-008-9147-z.

[18] M. Bhattacharya and J. Astola, "Multiplierless implementation of recursive digital filters using a class of low sensitivity structures," in *Sixth International, Symposium on 2001 Signal Processing and its Applications*, vol. 2, Kuala Lumpur, Malaysia, Aug. 13–16, 2001, pp. 611–614. DOI: 10.1109/ISSPA.2001.950219.

[19] S. J. Billman, "Design of a low power and area efficient digital down converter and SINC filter in CMOS 90-nm technology," Master's thesis, Dept. of Elect. Eng., Wright State University, USA, 2011. [Online]. Available: http://etd.ohiolink.edu/send-pdf.cgi/Billman%20Steven%20John.pdf?wright1307746437.

[20] Bindiya T. S., V. Satish Kumar, and E. Elias, "Design of low power and low complexity multiplier-less reconfigurable non-uniform channel filters using genetic algorithm," *Global Journal of researches in engineering Electrical and electronics engineering*, vol. 12, no. 6, pp. 7–19, 2011. [Online]. Available: https://globaljournals.org/GJRE_Volume12/2-Design-of-Low-Power-and-Low.pdf.

[21] M. Blok and M. Sac, "Variable fractional delay filter design using a symmetric window," *Circuits, Systems, and Signal Processing*, vol. 33, no. 10, pp. 3223–3250, May 2014. DOI: 10.1007/s00034-014-9803-8.

[22] S. Bou-Sleiman and M. Ismail, "RF built-in-self-calibration," in *Built-in-Self-Test and Digital Self-Calibration for RF SoCs*, ser. SpringerBriefs in Electrical and Computer Engineering, Springer, 2012, pp. 73–86. DOI: 10.1007/978-1-4419-9548-3_5.

[23] R. Bregović and T. Saramäki, "A general-purpose optimization approach for designing two-channel FIR filter banks," *IEEE Trans. Signal Processing*, vol. 51, pp. 1783–1791, Jul. 2003. DOI: 10.1109/TSP.2003.812726.

[24] D. Brückmann, "Flexible digital receiver architecture with optimized components," *AEÜ–Int. J. Electron. Commun.*, vol. 55, no. 6, pp. 408–416, Dec. 2001. DOI: 10.1078/1434-8411-54100061.

[25] —, "Optimized decimation stages with lattice wave digital filters for a flexible digital receiver architecture," in *Proceedings EUROCON 2001*, Bratislava, Slovakia, Jul. 5–7, 2001.

[26] D. Brückmann, "Design and realization of continuous-time wave digital filters," in *Proc. IEEE Int. Symp. Circuits Syst.*, Seattle, WA, USA, May 18–21, 2008, pp. 2901–2904. DOI: 10.1109/ISCAS.2008.4542064.

[27] —, "Optimized digital receiver for flexible wireless terminals," in *IEEE Workshop on Signal Processing Advances in Wireless Communications*, Jun. 15–18, 2003, pp. 649–652. DOI: 10.1109/SPAWC.2003.1319041.

[28] —, "Optimized digital signal processing for flexible receivers," in *Proc. IEEE Int. Conf. Acoustics, Speech, and Signal Processing*, vol. 4, 2002, pp. 3764–3767. DOI: 10.1109/ICASSP.2002.5745475.

[29] D. Brückmann and L. Bouhrize, "Filter stages for a high-performanace reconfigurable radio receiver with minimum system delay," in *Proc. IEEE Conf. Acoust., Speech, Signal Process.*, vol. 2, Honolulu, HI, U.S.A., May 15–20, 2007, pp. 117–120. DOI: 10.1109/ICASSP.2007.366186.

[30] —, "Filter stages for a high-performanace reconfigurable radio receiver with minimum system delay," in *Proc. IEEE Int. Conf. Acoustics, Speech, and Signal Processing*, Honolulu, Hawaii, USA, May 15–20, 2008, pp. 117–120. DOI: 10.1109/ICASSP.2007.366186.

[31] A. Burian, "Reduced-complexity code synchronization in multipath channels for boc-modulated cdma signals with applications in galileo and modernized gps systems," Dr. Tech. dissertation, Dept. of Commun. Eng., Tampere Univ. of Tech, Finland, Tampere, Finland, Oct. 2009. [Online]. Available: http://dspace.cc.tut.fi/dpub/bitstream/123456789/6093/1/burian.pdf.

[32] A. Burian, E. S. Lohan, V. Lehtinen, and M. Renfors, "Complexity considerations for unambiguous acquisition of galileo signals," in *Proc. 3rd Workshop on Positioning, Navigation and communication (WPNC'06)*, Hannover, Germany, 2006, pp. 65–73. [Online]. Available: http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.80.8581&rep=rep1&type=pdf.

[33] M.-A. Cantin, "Méthode de détermination automatique de la taille des chemins de données," PhD thesis, Université de Montréal, École Polytechnique de Montréal, 2005.

[34] M.-A. Cantin, Y. Savaria, and P. Lavoie, "A comparison of automatic word length optimization procedures," in *Proc. IEEE Int. Symp. Circuits Syst.*, Scottsdale, Arizona, May 26–29, 2002, pp. 612–615. DOI: 10.1109/ISCAS.2002.1011427.

[35] M.-A. Cantin, Y. Savaria, D. Prodanos, and P. Lavoie, "A metric for automatic word-length determination of hardware datapaths," *IEEE Trans. Computer-Aided Design*, vol. 25, no. 10, Oct. 2006. DOI: 10.1109/TCAD.2005.862733.

[36] —, "An automatic word length determination method," in *Proc. IEEE Int. Symp. Circuits Syst.*, Sydney, Australia, May 6–9, 2001, pp. 53–56. DOI: 10.1109/ISCAS.2001.921982.

[37] J. J. D. Carmona, *Diseño y aplicación de filtros de retraso fraccionario*, Lecture series by the Red CUDI System of Higher Education Technology, Oct. 28, 2011. [Online]. Available: http://www.cudi.mx/Feventos/F2011/FSNET_Javier_Diaz.pdf.

[38] M. Caus, A. I. Perez-Neira, and A. Kliks, "Characterization of the effects of multi-tap filtering on FBMC/OQAM systems," *EURASIP Journal on Advances in Signal Processing*, vol. 84, 2014. DOI: 10.1186/1687-6180-2014-84.

[39] C.-H. Chan, S. C. Pei, and J.-J. Shyu, "A new method for least-squares and minimax group-delay error design of allpass variable fractional-delay digital filters," *EURASIP J. Advances in Signal Process.*, vol. 2010, Article ID 976913, 10 pages, 2010. DOI: 10.1155/2010/976913.

[40] S. C. Chan and K. S. Yeung, "On the application of variable digital filters (VDF) to the realization of software radio receivers," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. III, Bangkok, Thailand, May 25–28, 2003, pp. 562–565. DOI: 10.1109/ISCAS.2003.1205081.

[41] A. Chandra and S. Chattopadhyay, "A novel approach for coefficient quantization of low-pass finite impulse response filter using differential evolution algorithm," *Signal, Image and Video Processing*, vol. 8, no. 7, pp. 1307–1321, Jul. 2012. DOI: 10.1007/s11760-012-0359-4.

[42] A. Chandra and S. Chattopadhyay, "A novel approach for coefficient quantization of low-pass finite impulse response filter using differential evolution algorithm," *Signal, Image and Video Processing*, vol. 8, no. 7, pp. 1307–1321, Oct. 2014. DOI: 10.1007/s11760-012-0359-4.

[43] —, "Canonic signed digit based design of multiplier-less FIR filter using self-organizing random immigrants genetic algorithm," *Int. J. Artificial Intelligence & Applications*, vol. 4, no. 4, pp. 21–34, Jul. 2013. DOI: 10.5121/ijaia.2013.4403.

[44] A. Chandra and S. Chattopadhyay, "Design optimisation of powers-of-two FIR filter using self-organising random immigrants GA," *Signal, Image and Video Processing*, vol. 102, no. 1, Mar. 2015. DOI: 10.1080/00207217.2014.938311.

[45] A. Chandra and S. Chattopadhyay, "Differential evolution based design of multiplier-less FIR filter using canonical signed digit representation," in *Int. Conf. Communications, Devices and Intelligent Systems*, Kolkata, India, 2012, pp. 425–428. DOI: 10.1109/CODIS.2012.6422229.

[46] A. Chandra and S. Chattopadhyay, "Novel approach of designing multiplier-less finite impulse response filter using differential evolution algorithm," *Int. J. Intelligent Systems and Application*, vol. 4, no. 4, pp. 54–52, Apr. 2012. [Online]. Available: http://www.mecs-press.org/ijisa/ijisa-v4-n4/IJISA-V4-N4-8.pdf.

[47] A. Chandra and S. Chattopadhyay, "Novel approach of designing multiplier-less finite impulse response filter using differential evolution algorithm," *Int. J. Intelligent Systems and Applications*, vol. 4, no. 4, pp. 54–62, Apr. 2012. DOI: 10.5815/ijisa.2012.04.08.

[48] —, "Novel design strategy of multiplier-less low-pass finite impulse response filter using self-organizing random immigrants genetic algorithm," *Signal, Image and Video Processing*, vol. 8, no. 3, pp. 507–522, Mar. 2014. DOI: 10.1007/s11760-013-0494-6.

[49] A. Chandra and S. Chattopadhyay, "Role of mutation strategies of differential evolution algorithm in designing hardware efficient multiplier-less low-pass FIR filter," *J. Multimedia*, vol. 7, no. 5, pp. 353–363, Oct. 2012. DOI: 10.4304/jmm.7.5.353-363.

[50] A. Chandra and S. Chattopadhyay, "Supremacy of differential evolution algorithm in designing multiplier-less low-pass fir filter," *Int. J. Electrical, Electronic Science and Engineering*, vol. 8, no. 2, pp. 120–129, 2014. [Online]. Available: http://waset.org/publication/Supremacy-of-Differential-Evolution-Algorithm-in-Designing-Multiplier-Less-Low-Pass-FIR-Filter/9997723.

[51] A. Chandra and S. Chattopadhyay, "Variants of genetic algorithm for efficient design of multiplier-less finite impulse response digital filter," in *Encyclopedia of Information Science and Technology*, M. Khosrow-Pour, Ed., IGI Global, 2015, pp. 1304–1313. DOI: 10.4018/978-1-4666-5888-2.ch124.

[52] M.-H. Chang, "Design of variable digital filters," Master's thesis, Dept. of Electrical Eng., National University of Kaohsiung, Taiwan, 2010.

[53] Y.-J. Cheng, "Design of high-level FIR filter synthesizer," Master's thesis, Dept. Electr. Eng., National Chiao Tung Univ., Taiwan, 2003.

[54] S. Chowdhary and M. M. Sarde, "Review of various optimization techniques for FIR filter design," *Int. J. Advanced Research in Electrical, Electronics, Instrumentation Eng.*, vol. 3, no. 1, pp. 6566–6571, Jan. 2014. [Online]. Available: http://www.ijareeie.com/upload/2014/january/14_Review.pdf.

[55] C.-C. Chua, B.-H. Gwee, and J. S. Chang, "A low-voltage micropower asynchronous multiplier for a multiplierless FIR filter," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 5, Bangkok, Thailand, May 25, 2003–May 28, 2004, pp. 381–384. DOI: 10.1109/ISCAS.2003.1206287.

[56] F. Cruz-Roldan, P. Amo-Lopez, S. Maldonado-Bascon, and S. S. Lawson, "An efficient and simple method for designing prototype filters for cosine-modulated pseudo-QMF banks," *IEEE Signal Processing Lett.*, vol. 9, no. 1, pp. 29–31, Jan. 2002. DOI: 10.1109/97.988722.

[57] H. H. Dam, "Design of allpass variable fractional delay filter," *IEEE Trans. Signal Processing*, vol. 59, no. 12, pp. 6240–6244, Dec. 2011. DOI: 10.1109/TSP.2011.2165951.

[58] —, "Variable fractional delay filter with sub-expression coefficients," *Int. J. Innovative Computing, Information and Control*, vol. 9, no. 7, pp. 2995–3003, 2013. [Online]. Available: www.ijicic.org/ijicic-12-05001.pdf.

[59] H. H. Dam, A. Cantoni, K. L. Teo, and S. Nordholm, "FIR variable digital filter with signed power-of-two coefficients," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 5, pp. 1348–1357, Jun. 2007. DOI: 10.1109/TCSI.2007.897775.

[60] H. H. Dam and K. L. Teo, "Allpass VFD filter design," *IEEE Trans. Signal Processing*, vol. 58, no. 8, pp. 4432–4436, Aug. 2010. DOI: 10.1109/TSP.2010.2048316.

[61] S. J. Darak, S. Dhabu, C. Moy, H. Zhang, J. Palicot, and A. P. Vinod, "Low complexity and efficient dynamic spectrum learning and tunable bandwidth access for heterogeneous decentralized cognitive radio networks," *Digital Signal Processing*, Dec. 2014. DOI: 10.1016/j.dsp.2014.12.001.

[62] L. C. R. de Barcellos, P. S. R. Diniz, and S. L. Netto, "A generalized oversampled structure for cosine-modulated transmultiplexers and filter banks," *Circuits, Syst., Signal Process.*, vol. 25, no. 2, pp. 131–151, Apr. 2006. DOI: 10.1007/s00034-005-2501-9.

[63] T.-B. Deng, "Generalized WLS method for designing allpass variable fractional-delay digital filters," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 10, pp. 2207–2220, Oct. 2009. DOI: 10.1109/TCSI.2009.2015213.

[64] —, "Non-iterative WLS design of allpass variable fractional-delay digital filters," in *Proc. IEEE Int. Symp. Circuits Syst.*, Kobe, Japan, 2005, pp. 504–507. DOI: 10.1109/ISCAS.2005.1464635.

[65] —, "Noniterative WLS design of allpass variable fractional-delay digital filters," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 2, pp. 358–371, Feb. 2006. DOI: 10.1109/TCSI.2005.854406.

[66] P. K. Devi and R. S. Bhuvaneshwaran, "Polyphase wideband channelisation architecture for cognitive radio," *Int. J. Science and Research Technology*, vol. 1, no. 5, pp. 1–6, 2014. [Online]. Available: {http://www.ijsrt.com/Documents/Volumes/Vol1\%20iss5/ijsrt\%20v1\%20i5\%20(2)\%20nd.pdf}.

[67] J. Diaz-Carmona and G. J. Dolecek, "Fractional delay digital filters," in *Applications of MATLAB in Science and Engineering*, T. Michałowski, Ed., InTech, 2011, pp. 247–272, ISBN: 978-953-307-708-6. [Online]. Available: http://www.intechopen.com/articles/show/title/fractional-delay-digital-filters.

[68] G. J. Dolecek and S. K. Mitra, "A new two-stage CIC-based decimation filter," in *Proc. IEEE Int. Symp. Image, Signal Process., Analysis*, Istanbul, Turkey, 2007, pp. 218–223. DOI: 10.1109/ISPA.2007.4383693.

[69] S. A. van Dorp Skogstad, "Methods and technologies for using body motion for real-time musical interaction," PhD thesis, Faculty of Mathematics and Natural Sciences, University of Oslo, Sep. 2013. [Online]. Available: http://urn.nb.no/URN:NBN:no-41124.

[70] A. J. S. Dutra, L. Lovisolo, E. A. B. da Silva, and P. S. R. Diniz, "Successive approximation FIR filter design," in *Proc. IEEE Int. Symp. Circuits Syst.*, Rio de Janeiro, Brazil, May 15–18, 2011, pp. 149–152. DOI: 10.1109/ISCAS.2011.5937523.

[71] A. Eghbali and H. Johansson, "Complexity reduction in low-delay Farrow-structure-based variable fractional delay FIR filters utilizing linear-phase subfilters," in *Proc. Euro. Conf. Circuit Theory Design*, Linköping, Sweden, Aug. 29–31, 2011, pp. 21–24. DOI: 10.1109/ECCTD.2011.6043300.

[72] A. Eghbali, H. Johansson, and T. Saramäki, "A method for the design of farrow-structure based variable fractional-delay fir filters," *Signal Processing*, vol. 93, no. 5, pp. 1341–1348, May 2012. DOI: 10.1016/j.sigpro.2012.11.010.

[73] F. C. El-Kareh, "Algoritmos genéticos aplicados ao projeto de filtros com coeficientes em soma de potências de dois," PhD thesis, Universidade do Estado do Rio de Janeiro, Brazil, Mar. 2011. [Online]. Available: http://www.pee.ufrj.br/teses/textocompleto/2010080601.pdf.

[74] P. Eneroth, "Joint filterbanks for echo cancellation and audio coding," *IEEE Trans. Speech Audio Processing*, vol. 11, no. 4, pp. 342–354, Jul. 2003. DOI: 10.1109/TSA.2003.814798.

[75] —, "Stereophonic acoustic echo cancellation: theory and implementation," No. 22, PhD thesis, Dept. of Electroscience, Lund Univ., Sweden, Feb. 2001. [Online]. Available: http://lup.lub.lu.se/luur/download?func=downloadFile&recordOId=41259&fileOId=1001945.

[76] Y.-Y. Fan, Z.-Q. Yu, Y.-J. Yuan, and G.-Y. Lü, "Design and implementation of a high performance class D power amplifier controller based on FPGA," *Systems Engineering and Electronics*, vol. 36, no. 4, pp. 630–636, Apr. 2014. DOI: 10.3969/j.issn.1001-506X.2014.04.04.

[77] S. F. Fard, A. Alimohammad, B. Cockburn, and C. Schlegel, "A single FPGA filter-based multipath fading emulator," in *Proc. IEEE Conf. on Global Telecommun.*, Honolulu, Hawaii, USA, 2009, pp. 4392–4396. [Online]. Available: http://dl.acm.org/citation.cfm?id=1811982.1812111.

[78] A. Farhang, N. Marchetti, and L. E. Doyle, "Low complexity transceiver design for GFDM," *arXiv:1501.02940 [cs.IT]*, 2015.

[79] U. Farooq, "Efficient architectural transformation of multirate recursive filters," PhD thesis, Univ. of Engineering and Technology, Taxila, Pakistan, 2008. [Online]. Available: prr.hec.gov.pk/Thesis/653S.pdf.

[80] H. Feng, Z. Yu, Z. Han, and F. Feng; "System level design of a digital audio class D power amplifier," in *Proc. Int. Conf. Multimedia Technol.*, Ningbo, China, 2010, pp. 1–5. DOI: 10.1109/ICMULT.2010.5631340.

[81] T. Fox and A. Carreira, "The design of low-cost fixed-point FIR digital filters using an improved local search," in *2003 IEEE Pacific Rim Conf. Commun., Computers and Signal Process.*, vol. 1, Victoria, BC, USA, Aug. 2003, pp. 249–252. DOI: 10.1109/PACRIM.2003.1235764.

[82] A. Francis and R. Cheriyan, "Filter centered nonisotropic fading channel archetypal for wireless system assessment," *Int. J. Innovative Research in Science, Engineering, and Technology*, vol. 3, no. 5, Jul. 2014. [Online]. Available: http://www.ijirset.com/upload/2014/special/iciaset/1_ashish_iciaset.pdf.

[83] A. Francis and R. Cheriyan, "Proficient envelope shaping filter for fading wireless channel estimation," in *Annual Int. Conf. Emerging Research Areas: Magnetics, Machines and Drives (AICERA/iCMMD), 2014*, Kottayam, India, India, 2014, pp. 1–4. DOI: 10.1109/AICERA.2014.6908265.

[84] A. Franck, K. Brandenburg, and U. Richter, "Efficient delay interpolation for wave field synthesis," in *AES 125th Int. Conv.*, San Francisco, CA, USA, Oct. 5, 2008–Oct. 8, 2007.

[85] T. Fujie, R. Ito, K. Suyama, and R. Hirabayashi, "A new heuristic signed-power of two term allocation approach for designing of FIR filters," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 4, May 25–28, 2003, pp. 285–288. DOI: 10.1109/ISCAS.2003.1205829.

[86] S. R. Gaikwad and G. Gawande, "Review: Design of highly efficient multirate digital filters," *Int. Journal of Engineering Research and Application*, vol. 3, no. 6, pp. 560–564, 2013. [Online]. Available: www.ijera.com/papers/Vol3_issue6/CR36560564.pdf.

[87] M. B. Gately, M. B. Yeary, and C. Y. Tang, "An algorithm for jointly optimizing quantization and multiple constant multiplication," *ACM Trans. Design Autom. Electr. Syst.*, vol. 17, no. 4, Oct. 2012. DOI: 10.1145/2348839.2348846.

[88] D. Gu, J. Hua, J. Wang, W. Kuang, and B. Sheng, "Comparative study of heuristic search algorithm in digital FIR filter design," in *2012 Int. Conf. on Wireless Commun. & Signal Process.*, Huangshan, China, 2012, pp. 1–5. DOI: 10.1109/WCSP.2012.6542857.

[89] O. Gustafsson, A. G. Dempster, K. Johansson, M. D. Macleod, and L. Wanhammar, "Simplified design of constant coefficient multipliers," *Circuits, Syst., Signal Process.*, vol. 25, no. 2, pp. 225–251, Apr. 2006. DOI: 10.1007/s00034-005-2505-5.

[90] O. Gustafsson, H. Johansson, and L. Wanhammar, "An MILP approach for the design of linear-phase FIR filters with minimum number of signed-power-of-two terms," in *Proc. Euro. Conf. Circuit Theory Design*, vol. 2, Espoo, Finland, Aug. 28–31, 2001, pp. 217–220. [Online]. Available: http://www.es.isy.liu.se/publications/papers_and_reports/2001/oscarg_ECCTD01_R2390.pdf.

[91] —, "MILP design of frequency-response masking FIR filters with few SPT terms," in *Proc. 2004 IEEE Int. Symp. Control., Commun., Signal Process.*, Hammamet, Tunisia, Nov. 21–24, 2004, pp. 405–408. DOI: 10.1109/ISCCSP.2004.1296314.

[92] O. Gustafsson and F. Qureshi, "Addition aware quantization for low complexity and high precision constant multiplication," *IEEE Signal Processing Lett.*, vol. 17, no. 2, pp. 173–176, Feb. 2010. DOI: 10.1109/LSP.2009.2036384.

[93] O. Gustafsson and L. Wanhammar, "Design of linear-phase FIR filters with minimum Hamming distance," in *IEEE Nordic Signal Processing Symp.*, Hurtigruten, Norway, Oct. 4–7, 2002. [Online]. Available: http://www.ux.uis.no/norsig/norsig2002/Proceedings/papers/cr1052.pdf.

[94] —, "Design of reduced complexity linear-phase polyphase FIR filters using mixed integer linear programming," in *Swedish System-on-Chip Conf.*, Båstad, Sweden, May 13–14, 2004. [Online]. Available: http://www.es.isy.liu.se/publications/papers_and_reports/2004/oscarg_ssocc2004.pdf.

[95] —, "Low-complexity and high-speed constant multiplications for digital filters using carry-save arithmetic," in *Digital Filters*, F. P. G. Márquez, Ed., InTech, 2011. [Online]. Available: http://www.intechopen.com/articles/show/title/low-complexity-and-high-speed-constant-multiplications-for-digital-filters-using-carry-save-arithmet.

[96] E. Gutiérrez, J. A López-Salcedo, and G. Seco-Granados, "Systematic design of transmitter and receiver architectures for flexible filter bank multi-carrier signals," *EURASIP Journal on Advances in Signal Processing*, 2014, 2014:103. DOI: 10.1186/1687-6180-2014-103.

[97] M. Hallal, B. Swaked, and L. Albasha, "Preliminary all digital channel filter design for LTE-advanced software radio implementation," in *Int. Conf. Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*, Abu Dhabi, United Arab Emirates, 2013, pp. 173–175. DOI: 10.1109/DTIS.2013.6527802.

[98] J.-H. Han, "Research on the area efficient and high performance digital FIR filter design," PhD thesis, Dept. of Elect. Eng., Korea Advanced Institute of Science and Technology, Daejeon, Korea, 2010.

[99] D. Harris, "Computationally efficient variable linear phase filters," Master's thesis, Univ. Miami, Florida, U.S.A, 2007. [Online]. Available: http://muerocks.wikispaces.com/file/view/HarrisDraft3-01-07.pdf.

[100] E. Hermanowicz and H. Johansson, "A complex variable fractional-delay FIR filter structure," *IEEE Trans. Circuits Syst. II*, vol. 54, no. 9, pp. 785–789, Sep. 2007. DOI: 10.1109/TCSII.2007.900349.

[101] Y. da Huang, "Design of variable digital filters," Master's thesis, National Univ. of Kaohsiung, Taiwan, 2008. [Online]. Available: http://ethesys.nuk.edu.tw/ETD-db/ETD-search/getfile?URN=etd-0718108-155103&filename=etd-0718108-155103.pdf.

[102] Z. Hui and K. H. Keung, "Design of 1-D stable variable fractional delay IIR filters," *IEEE Trans. Circuits Syst. II*, vol. 54, no. 1, pp. 86–90, Jan. 2007. DOI: 10.1109/TCSII.2006.882802.

[103] R. Ito, T. Fujie, K. Suyama, and R. Hirabayashi, "A new heuristic approach for design of FIR filters with SP2 coefficients in a min-max sense," in *Proc. 7th Int. Conf. on Signal Process.*, vol. 1, Beijing, China, Aug. 31–Sep. 4, 2004, pp. 81–84. DOI: 10.1109/ICOSP.2004.1452586.

[104] —, "Design methods of FIR filters with signed power of two coefficients using a new linear programming relaxation with triangle inequalities," *Int. J. of Innovative Comput., Inform. Control*, vol. 2, no. 2, pp. 441–448, Apr. 2006. [Online]. Available: http://www.ijicic.org/04-034-1.pdf.

[105] —, "New design method of FIR filters with SP2 coefficients based on a new linear programming relaxation with triangle inequalities," in *Proc. Euro. Conf. Circuit Theory Design*, vol. II, Toulouse, France, Sep. 3–6, 2002, pp. 615–618. [Online]. Available: www.eurasip.org/Proceedings/Eusipco/2002/articles/paper303.pdf.

[106] —, "New design methods of FIR filters with signed power of two coefficients based on a new linear programming relaxation with triangle inequalities," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 1, Scottsdale, Arizona, May 26–29, 2002, pp. 813 –816. DOI: 10.1109/ISCAS.2002.1009965.

[107] R. Ito and R. Hirabayashi, "Design of FIR filter with discrete coefficients based on semi-infinite linear programming method," *Pacific J. Optimization*, vol. 3, no. 1, pp. 53–86, Jan. 2007. [Online]. Available: http://www.ybook.co.jp/online/pjoe/vol3/pjov3n1p73.html.

[108] Y.-W. Jiang, S.-Y. Liu, and X.-W. Mu, "Branch-and-bound algorithm for design of FIR filters with discrete coefficients," *Computer Engineering and Applications*, vol. 45, no. 13, pp. 72–74, 2009. [Online]. Available: http://www.ceaj.org/jsjgc/qikan/public/tjdjl_en.asp?wenjianming=8090983&houzhui=.pdf&id=9683.

[109] H. Johansson, O. Gustafsson, K. Johansson, and L. Wanhammar, "Adjustable fractional-delay FIR filters using the Farrow structure and multirate techniques," in *Proc. IEEE Acia Pacific Conf. Circuits Syst.*, Singapore, Dec. 4–7, 2006, pp. 1057–1060. DOI: 10.1109/APCCAS.2006.342270.

[110] H. Johansson, "Farrow-structure-based reconfigurable bandpass linear-phase FIR filters for integer sampling rate conversion," *IEEE Trans. Circuits Syst. II*, vol. 58, no. 1, pp. 46–50, Jan. 2011. DOI: 10.1109/TCSII.2010.2092826.

[111] —, "Fractional-delay and supersymmetric Mth-band linear-phase FIR filters utilizing partially symmetric and antisymmetric impulse responses," *IEEE Trans. Circuits Syst. II*, vol. 59, no. 6, pp. 366–370, Jun. 2012. DOI: 10.1109/TCSII.2012.2195060.

[112] —, "On FIR filter approximation of fractional-order differentiators and integrators," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 3, no. 3, pp. 404–415, Sep. 2013. DOI: 10.1109/JETCAS.2013.2273853.

[113] —, "Two classes of frequency-response masking linear-phase FIR filters for interpolation and decimation," *Circuits, Syst., Signal Process.*, vol. 25, no. 2, pp. 175–200, Apr. 2006. DOI: 10.1007/s00034-005-2503-7.

[114] H. Johansson and A. Eghbali, "Two polynomial FIR filter structures with variable fractional delay and phase shift," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 5, pp. 1355–1365, 2014. DOI: 10.1109/TCSI.2014.2309863.

[115] H. Johansson and O. Gustafsson, "Two-rate based structures for computationally efficient wide- band FIR systems," in *Digital Filters and Signal Processing*, F. P. G. Márquez and N. Zaman, Eds., InTech, 2013, pp. 189–211, ISBN: 978-953-51-0871-9. DOI: 10.5772/52198. [Online]. Available: http://www.intechopen.com/download/pdf/40215.

[116] H. Johansson and E. Hermanowicz, "Two-rate based low-complexity variable fractional-delay FIR filter structures," *IEEE Trans. Circuits Syst. I*, vol. 60, no. 1, pp. 136–149, Jan. 2013. DOI: 10.1109/TCSI.2012.2215697.

[117] H. Johansson and L. Wanhammar, "High-speed recursive digital filters based on the frequency-response masking approach," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 48–61, Jan. 2000. DOI: 10.1109/82.818894.

[118] M. Joliveau, M. Gendreau, F. Gagnon, and C. Thibeault, "Low complexity low power non-recursive digital filters with unconstrained topology," in *Proc. Euro. Conf. Circuit Theory and Design*, Linköping, Sweden, Aug. 29–31, 2011, pp. 865–868. DOI: 10.1109/ECCTD.2011.6043821.

[119] I. H. H. Jørgensen, P. Pracný, and E. Bruun, "Hardware-efficient implementation of half-band IIR filter for interpolation and decimation," *IEEE Trans. Circuits Syst. II*, vol. 60, no. 12, pp. 892–896, Dec. 2013. DOI: 10.1109/TCSII.2013.2285975.

[120] S. Jošilo, M. Pejović, B. Dorđević, M. Narandžić, and S. Nedić, "Multicarrier waveforms with I/Q staggering: Uniform and nonuniform FBMC formats," *EURASIP Journal on Advances in Signal Processing*, no. 167, Nov. 2014. DOI: 10.1186/1687-6180-2014-167.

[121] S. Jošilo, M. Pejović, and S. Nedić, "Non-uniform FBMC – A pragmatic approach," in *Proc. Int. Symp. Wireless Communication Systems 2013*, Ilmenau, Germany, 2013, pp. 36–40.

[122] S. Jošilo, M. Pejović, B. Đorđević, Narandžić, and S. Nedić, "Multicarrier waveforms with I/Q staggering – Uniform and non-uniform FBMC," *EURASIP J. Advances in Signal Process.*, 2014.

[123] G. Jovanovic-Dolecek, M. M. Alvarez, and M. Martinez, "One simple method for design of multiplierless FIR filters," *J. of Appl. Research and Technol.*, vol. 3, no. 2, pp. 125–138, Aug. 2005. [Online]. Available: http://www.redalyc.org/pdf/474/47420227005.pdf.

[124] G. Jovanovic Dolecek, "Design and applications of digital filters," in *Encyclopedia of Information Science and Technology*, P. Margherita, Ed., Hershey, PA: Information Science Reference, 2009, pp. 1016–1023. DOI: 10.4018/978-1-60566-026-4.ch162.

[125] —, "Digital filters," in *Encyclopedia of Multimedia Technology and Networking*, M. Pagani, Ed., Hershey, PA: Information Science Reference, 2009, pp. 364–372. DOI: 10.4018/978-1-60566-014-1.ch050.

[126] G. Jovanovic-Dolecek, M. M. Alvarez, and M. A. Martinez, "One simple method for design of multiplierless FIR filters," in *Innovations Through Information Technology*, M. Khosrow-Pour, Ed., IGPPress, 2004, pp. 593–594. DOI: 10.4018/978-1-59140-261-9.ch151.

[127] G. Jovanović-Dolecek and S. K. Mitra, "Low sensitivity second-order bandpass digital filter structure," *Electron. Lett.*, vol. 38, no. 15, pp. 858–860, Jul. 2002. DOI: 10.1049/el:20020617.

[128] M. Kapar, C. Ö. Solmaz, and A. H. Kayran, "Optimization of FIR filters synthesized using the generalized one-stage frequency-response masking approach," in *Proc. 14th IEEE Signal Process. and Commun. Appl.*, Antalya, Turkey, 2006, pp. 1–4. DOI: 10.1109/SIU.2006.1659726.

[129] —, "Optimization of FIR filters synthesized using the generalized one-stage frequency-response masking approach," in *Proc. Euro. Conf. Circuit Theory Design*, Florence, France, 2006, pp. 1–4. [Online]. Available: http://www.eurasip.org/Proceedings/Eusipco/Eusipco2006/HTML/papers/1568982062.pdf.

[130] H. Kaur, A. Kumar, R. Kaur, D. Singh, and S. Kumar, "Investigation on optimization approach to digital filters," *Invertis Journal of Science & Technology*, vol. 4, no. 2, pp. 65–71, 2011. [Online]. Available: http://invertisuniversity.ac.in/Media/Journals/4PIUHO.pdf.

[131] A. B. Kharate and P. R. Gumble, "Design of 6 tap FIR filter using VLSI for low power MAC," in *International Conference on Emerging Trends in Engineering and Techno - Sciences*, Coimbatore, India, 2013, pp. 48–52.

[132] S. M. Kilambi, B. Nowrouzian, and Y. Wu, "A novel diversity-controlled genetic algorithm for rapid optimization of bandpass FRM FIR digital filters over CSD multiplier coefficient space," *Circuits, Syst., Signal Process.*, 2008. DOI: 10.1007/s00034-008-9045-8.

[133] J. Kleider and C. Steenhoek, "On the performance of variable fractional delay arbitrary sample rate conversion for digital signals," in *2014 IEEE Military Communications Conference (MILCOM)*, 2014, pp. 724–730. DOI: 10.1109/MILCOM.2014.126.

[134] —, "On the performance of variable fractional delay arbitrary sample rate conversion for digital signals," in *IEEE Military Communications Conference*, Baltimore, MD, USA, 2014, pp. 724–730. DOI: 10.1109/MILCOM.2014.126.

[135] B. Y. Kong and I.-C. Park, "FIR filter synthesis based on interleaved processing of coefficient generation and multiplier-block synthesis," *IEEE Trans. Computer-Aided Design*, vol. 31, no. 8, pp. 1169–1179, Aug. 2012. DOI: 10.1109/TCAD.2012.2190826.

[136] S. Koshita, K. Miyoshi, M. Abe, and M. Kawamata, "High-performance variable band-pass/band-stop state-space digital filters using gramian-preserving frequency transformation," *Digit. Signal Process.*, vol. 27, pp. 175–184, Jan. 2014. DOI: 10.1016/j.dsp.2014.01.003.

[137] W. Kuang, J. Hua, Z. Gao, C. Ruan, and L. Meng, "Comparative study of frequency domain constraints on FIR filter design by frequency sampling," in *Int. Conf. Automatic Control and Artificial Intelligence (ACAI 2012)*, Xiamen, China, 2012, pp. 659–663. DOI: 10.1049/cp.2012.1064.

[138] Y.-T. Kuo, T.-J. Lin, and C.-W. Liu, "Complexity-aware quantization and lightweight VLSI implementation of FIR filters," *2011*, EURASIP J. Advances in Signal Process. DOI: 10.1155/2011/357906.

[139] C.-M. Lee, "The dynamic analysis of evolutionary algorithm and its application to the design of digital filters," PhD thesis, Dept. Electr. Eng., National Central Univ. of Taiwan, Taiwan, Dec. 2005. [Online]. Available: http://thesis.lib.ncu.edu.tw/ETD-db/ETD-search/view_etd?URN=90541015#anchor.

[140] W. R. Lee, L. Caccetta, and V. Rehbock, "Optimal design of all-pass variable fractional-delay digital filters," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 5, pp. 1248–1256, Jun. 2008. DOI: 10.1109/TCSI.2008.916686.

[141] W. R. Lee, L. Caccetta, K. L. Teo, and V. Rehbock, "A unified approach to multistage frequency-response masking filter design using the WLS technique," *IEEE Trans. Signal Processing*, vol. 54, no. 9, pp. 3459–3467, Sep. 2006. DOI: 10.1109/TSP.2006.877652.

[142] —, "A weighted least squares approach to the design of FIR filters synthesized using the modified frequency response masking structure," *IEEE Trans. Circuits Syst. II*, vol. 53, no. 5, pp. 379–383, May 2006. DOI: 10.1109/TCSII.2005.862282.

[143] W. R. Lee, V. Rehbock, K. L. Teo, and L. Caccetta, "Frequency-response masking based FIR filter design with power-of-two coefficients and optimum PWR," in *Proc. IEEE Int. Conf. Electr. Circuits Syst. (ICECS 2002)*, vol. III, Dubrovnik, Croatia, Sep. 15–18, 2002, pp. 1175–1178. DOI: 10.1109/ICECS.2002.1046462.

[144] —, "Frequency-response masking based FIR filter design with power-of-two coefficients and suboptimum PWR," *J. Circuits, Syst., Computers*, vol. 12, no. 5, pp. 591–599, Oct. 2003. DOI: 10.1142/S0218126603001045.

[145] J. Li, "Design of approximately flat group delay selective IIR filters based on wave digital allpass filters," Master's thesis, Dept. of Elect. and Computer Eng., University of Manitoba, Winnipeg, Manitoba, Canada, 2002. [Online]. Available: http://hdl.handle.net/1993/19674.

[146] Y. Lian, "Complexity reduction for FRM-based FIR filters using the prefilter-equalizer technique," *Circuits, Syst., Signal Process.*, vol. 22, no. 2, pp. 137–155, Mar. 2003. DOI: 10.1007/s00034-004-7024-2.

[147] Y. C. Lim, "Fourier series optimization: Minimizing the number of nonzero coefficients," in *Proc. Int. Conf. Optimization and Control*, Guiyang, China, Jul. 18–18, 2010, pp. 261–276. [Online]. Available: http://yli-kaakinen.fi/publications/CSC03/Lim,%20Y.%20C.%20(2010,%20ICOCO)%20Fourier%20series%20optimization%20-%20Minimizing%20the%20number%20of%20nonzero%20coefficients.pdf.

[148] Y. C. Lim and R. Yang, "On the synthesis of very sharp decimators and interpolators using the frequency-response masking technique," *IEEE Trans. Signal Processing*, vol. 53, no. 4, pp. 1387–1397, Apr. 2005. DOI: 10.1109/TSP.2005.843743.

[149] Y. C. Lim, Y. J. Yu, K. L. Teo, and T. Saramäki, "Frm-based FIR filters with minimum coefficient sensitivities," in *Proc. IEEE Int. Symp. Circuits Syst.*, New Orleans, LA, USA, May 27–30, 2007, pp. 2962–2965. DOI: 10.1109/ISCAS.2007.377871.

[150] Y. C. Lim and Y. J. Yu, "Synthesis of very sharp Hilbert transformer using the frequency-response masking technique," *IEEE Trans. Signal Processing*, vol. 53, no. 7, pp. 2595–2597, Jul. 2005. DOI: 10.1109/TSP.2005.849206.

[151] Y. C. Lim, Y. J. Yu, and T. Saramäki, "FRM approach for Hilbert tranformer synthesis," in *Proc. Int. Conf. Inform. Technol. & Appl.*, Harbin, China, Jan. 15–18, 2007, pp. 670–673. [Online]. Available: http://yli-kaakinen.fi/publications/CSC03/Yu07_ICITA.pdf.

[152] —, "Optimum masking levels and coefficient sparseness for Hilbert transformers and half-band filters designed using the frequency-response masking technique," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 11, pp. 2444–2453, Nov. 2005. DOI: 10.1109/TCSI.2005.853518.

[153] Y. C. Lim, Y. J. Yu, K. L. Teo, and T. Saramäki, "FRM-based FIR filters with optimum finite word-length performance," *IEEE Trans. Signal Processing*, vol. 55, no. 6, pp. 2914–2924, Jun. 2007. DOI: 10.1109/TSP.2007.893965.

[154] Y. C. Lim, Y. J. Yu, H. Q. Zheng, and S. W. Foo, "FPGA implementation of digital filters synthesized using the FRM technique," *Circuits, Syst., Signal Process.*, vol. 22, no. 2, pp. 211–218, Mar. 2003. DOI: 10.1007/s00034-004-7027-z.

[155] S.-H. Lin, "Design of tunable one-dimensional and two-dimensional digital comb filters," Master's thesis, National Taiwan University, Taiwan, 2009.

[156] Z. Lin and Y. Liu, "FRM filter design with group delay constraint using second-order cone programming," in *Proc. IEEE Int. Symp. Circuits Syst.*, New Orleans, LA, USA, May 27–30, 2007, pp. 2954–2957. DOI: 10.1109/ISCAS.2007.377869.

[157] Y. Liu and Z. Lin, "Optimal design of frequency-response masking filters with reduced group delays," *IEEE Trans. Circuits Syst.*, vol. 55, no. 6, pp. 1560–1570, Jul. 2008. DOI: 0.1109/TCSI.2008.916619.

[158] E. S. Lohan, A. Burian, and M. Renfors, "Low-complexity unambiguous acquisition methods for BOC-modulated CDMA signals," *Int. J. Satellite Communications and Networking*, vol. 26, no. 6, pp. 503–522, Oct. 2008. DOI: 10.1002/sat.922.

[159] P. Löwenborg, E. Elias, H. Johansson, and L. Wanhammar, "Two-channel IIR/FIR filter banks with very low-complexity analysis or synthesis filters: Finite wordlength effects," in *Proc. 44th IEEE 2001 Midwest Symp. Circuits Syst.*, vol. 1, Dayton, OH, USA, Aug. 14–17, 2001, pp. 126–129. DOI: 10.1109/MWSCAS.2001.986131.

[160] C.-K. Lu and S. Summerfield, "Design and VLSI implementation of QMF banks," *IEE Proc. Vis. Image Signal Process.*, vol. 151, no. 5, pp. 421–427, Oct. 2004. DOI: 10.1049/ip-vis:20040602.

[161] W.-S. Lu, "Design of FIR filters with discrete coefficients via sphere relaxation," in *Proc. IEEE Int. Symp. Circuits Syst.*, Island of Kos, Greece, May 21–24, 2006, pp. 2509–2512. DOI: 10.1109/ISCAS.2006.1693133.

[162] W.-S. Lu, "A unified approach for the design of 2-D digital filters via semidefinite programming," *IEEE Trans. Circuits Syst. I*, vol. 49, pp. 814–826, Jun. 2002. DOI: 10.1109/TCSI.2002.1010036.

[163] —, "Design of 2-D FIR filters with power-of-two coefficients: A semidefinite programming relaxation approach," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 2, Sydney, Australia, May 6–9, 2001, pp. 549–552. DOI: 10.1109/ISCAS.2001.921129.

[164] —, "Design of FIR digital filters with discrete coefficients via convex programming," in *Proc. IEEE Int. Symp. Circuits Syst.*, Kobe, Japan, May 23–26, 2005, pp. 1831–1834. DOI: 10.1109/ISCAS.2005.1464966.

[165] —, "Design of FIR filters with discrete coefficients: A semidefinite programming relaxation approach," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 2, Sydney, Australia, May 6–9, 2001, pp. 297–300. DOI: 10.1109/ISCAS.2001.921066.

[166] W.-S. Lu and T. Hinamoto, "Design of FIR filters with discrete coefficients via polynomial programming: Towards the global solution," in *Proc. IEEE Int. Symp. Circuits Syst.*, New Orleans, LA, USA, May 27–30, 2007, pp. 2048–2051. DOI: 10.1109/ISCAS.2007.378500.

[167] —, "Design of frequency-response-masking FIR filters using SOCP with coefficient sensitivity constraint," in *Proc. IEEE Int. Symp. Circuits Syst.*, Seattle, WA, USA, May 18–21, 2008, pp. 2442–2445. DOI: 10.1109/ISCAS.2008.4541949.

[168] W.-y. Luo, S.-p. Liu, L.-z. Zhang, and L. Jin, "A novel variable bandwidth FRM filter," *Journal of Circuits and Systems*, no. 6, 2009.

[169] B. Lutovac, "An application symbolic analysis for design efficient digital filters," in *11th Telecommunications Forum, TELFOR'2003*, Belgrade, Serbia, Nov. 25–26, 2003. [Online]. Available: http://www.telfor.rs/telfor2003/radovi/7-7.pdf.

[170] M. D. Lutovac and L. D. Milić, "Design of high-speed IIR filters based on elliptic minimal Q-factors prototype," in *Proc IEEE Conf. ETRAN*, Banja Vrucica, Yugoslav, Jun. 3–6, 2002. [Online]. Available: http://home.etf.rs/~lutovac/pdf/etan02lm.pdf.

[171] A. Martinez Jimenez, "Análisis de arquitecturas de multiplicadores digitales y su implementacion en fpga," Master's thesis, Intituto Politecnico Nacional, México, Sep. 2005. [Online]. Available: http://itzamna.bnct.ipn.mx:8080/dspace/bitstream/123456789/2641/1/448_2005_ESIME-CUL_MAESTRIA_alfredo_martinez.pdf.

[172] D. L. Maskell, J. Leiwo, and J. C. Patra, "The design of multiplierless FIR filters with a minimum adder step and reduced hardware complexity," in *Proc. IEEE Int. Symp. Circuits Syst.*, Island of Kos, Greece, May 21–24, 2006, pp. 605–608. DOI: 10.1109/ISCAS.2006.1692658.

[173] D. L. Maskell and A. P. Vinod, "Efficient multiplierless channel filters for multi-standard SDR," in *Proc. IEEE Int Conf. Computer and Information Technology*, Sydney, Australia, Jul. 8–11, 2008, pp. 237–242. DOI: 10.1109/CIT.2008.4594680.

[174] —, "Multiplierless multi-standard SDR channel filters," in *Proc. IEEE 2008 Int. Workshop on Multimedia Signal Process.*, Cairns, Australia, Oct. 8–11, 2008, pp. 815–819. DOI: 10.1109/MMSP.2008.4665186.

[175] D. L. Maskell, "Design of efficient multiplierless FIR filters," *IET Circuits, Devices, Syst.*, vol. 1, no. 2, pp. 175–180, Apr. 2007. DOI: 10.1049/iet-cds:20060201.

[176] D. L. Maskell and J. Leiwo, "Hardware-efficient fir filters with reduced adder step," *Electron. Lett.*, vol. 41, no. 22, pp. 1211–1213, Oct. 27, 2005. DOI: 10.1049/el:20052559.

[177] D. Mattera, M. Tanda, and M. Bellanger, "Performance analysis of some timing offset equalizers for FBMC/OQAM systems," *Signal Processing*, vol. 108, pp. 167–182, Mar. 2015. DOI: 10.1016/j.sigpro.2014.09.003.

[178] U. Meyer-Baese, G. Botella, D. E. T. Romero, and M. Kumm, "Optimization of high speed pipelining in FPGA-based FIR filter design using genetic algorithm," in *Proc. SPIE 8401, Independent Component Analyses, Compressive Sampling, Wavelets, Neural Net, Biosystems, and Nanoengineering X*, vol. 8401, Baltimore, Maryland, USA, May 2012. DOI: 10.1117/12.918934.

[179] L. Milić and M Lutovac, "Multiplierless IIR digital filters," *Nauka, Tehnika, Bezbednost*, vol. 11, no. 1, pp. 81–100, 2001.

[180] L. D. Milić, T. Saramäki, and Bregović, "Multirate filters: An overview," in *Proc. IEEE Asia Pacific Conf. on Circuits*, Singapore, Dec. 2006, pp. 914–917.

[181] L. D. Milić and M. D. Lutovac, "Efficient algorithm for the design of high-speed elliptic IIR filters," *AEÜ–Int. J. Electron. Commun.*, vol. 57, no. 4, pp. 255–262, 2003. DOI: 10.1078/1434-8411-54100168.

[182] A. T. Mingazin, "Finite wordlength coefficient digital filters based on allpass networks," in *Proc. DSPA*, vol. 1, Moscow, Russia, Mar. 28–30, 2010, pp. 108–111. [Online]. Available: www.radis.ru/articles/aming10r.pdf.

[183] —, "Improved synthesis of the two-channel perfect lattice filter banks with no multipliers," *Modern electronics*, no. 3, pp. 26–31, 2008. [Online]. Available: www.soel.ru/cms/f/?/369597.pdf.

[184] —, "Modification of the synthesis algorithm of digital filters based on phase circuits with finite wordlength coefficients," *Modern electronics*, no. 5, pp. 74–76, 2010. [Online]. Available: www.soel.ru/cms/f/?/434734.pdf.

[185] —, "Multiplierless two-channel perfect reconstruction lattice filter bank design using spectral factor selection," in *Int. Conf. Digital Signal Processing and its Applications (DSPA 2008)*, In Russian, vol. 1, 2008, pp. 129–96. [Online]. Available: http://www.radis.ru/articles/200803026.pdf.

[186] —, "Non-integer order in finite wordlength coefficient design of digital filters based on allpass networks," in *Proc. DSPA*, vol. 1, Moscow, Russia, Mar. 31–Apr. 2, 2010, pp. 120–121. [Online]. Available: http://www.radis.ru/articles/Thes19.pdf.

[187] —, "Synthesis of low complexity IIR filters," *Components & Technologies*, no. 11, pp. 58–62, 2013.

[188] —, "Synthesis of perfect lattice filter banks without multipliers," *The art electronics*, vol. 3, pp. 50–55, 2007. [Online]. Available: www.soel.ru/cms/f/?/351056.pdf.

[189] —, "The synthesis of digital filters for high-speed systems on-chip," *Digital signal processing*, no. 2, pp. 14–23, 2004, In russian. [Online]. Available: http://www.radis.ru/articles/Min04DSP.pdf.

[190] —, "Two examples of multiplierless perfect reconstruction lattice filter bank design," in *Int. Conf. Digital Signal Processing and its Applications (DSPA 2009)*, In Russian, vol. 1, 2009, p. 102.

[191] —, "Variation of initial parameters in design of multiplierless perfect reconstruction lattice FIR filter banks," in *Int. Conf. Digital Signal Processing and its Applications (DSPA 2007)*, In Russian, vol. 1, 2007, pp. 92–96. [Online]. Available: http://www.autex.spb.ru/pdf/dspa07-22.doc.

[192] —, "Variation of initial parameters of weighted Chebyshev approximation in multiplierless FIR filter design," in *Int. Conf. Digital Signal Processing and its Applications (DSPA 2005)*, vol. 1, Mar. 16, 2005–Mar. 18, 2003, pp. 56–59. [Online]. Available: www.radis.ru/articles/aming12e.pdf.

[193] A. Mohsen and R. Hofmann, "Power-aware scheduling for hard real-time embedded systems using voltage-scaling enabled architectures," in *15th Int. Workshop on Power and Timing Optimization and Simulation*, Leuven, Belgium, Sep. 21–23, 2005, pp. 127–136. DOI: 10.1007/11556930_14.

[194] S. T. N. Nguyen, "Design of two-band critically sampled rational rate filter banks with multiple regularity orders and associated discrete wavelet transforms," *IEEE Trans. Signal Processing*, vol. 60, no. 7, pp. 3863–3868, Jul. 2012. DOI: 10.1109/TSP.2012.2194711.

[195] H. Ohlsson, O. Gustafsson, and L. Wanhammar, "Arithmetic transformations for increased maximal sample rate of bit-parallel bireciprocal lattice wave digital filters," in *Proc. IEEE Int. Symp. Circuits Syst.*, Sydney, Australia, May 6–9, 2001. DOI: 10.1109/ISCAS.2001.921198.

[196] M. Olsson, "Contributions to frequency offset and time delay estimation," Linköping Studies Sci. Technol., Thesis. No. 1252, PhD thesis, Dept. of Electr. Eng., Linköping Univ., Sweden, May 2006. [Online]. Available: http://www.es.isy.liu.se/publications/theses/LiU-Tek-Lic-2006-M_Olsson.pdf.

[197] H.-q. Pan, S.-l. Tian, P. Ye, and H. Zeng, "An evaluation and calibration method for sampling time uniformity of high-speed parallel sampling systems," *ACTA Metrologica Sinica*, vol. 31, no. 4, 2010.

[198] H. Pan, S. Tian, and P. Ye, "An adaptive synthesis calibration method for time-interleaved sampling systems," *Metrol. Meas. Syst*, vol. XVII, no. 3, pp. 405–414, 2010. [Online]. Available: http://www.metrology.pg.gda.pl/full/2010/M&MS_2010_405.pdf.

[199] H. Pan, S. Tian, and Z. H. Ye Peng and, "Adaptive signal reconstruction for timing nonuniform of parallel sampling systems," *J. Electronic Measurement and Instrument*, vol. 24, no. 1, pp. 34–38, 2010. [Online]. Available: http://pub.chinasciencejournal.com/article/downArticle.action?articleid=11666&issn=1000-7105.

[200] S. Y. Park and N. I. Cho, "Design of signed powers-of-two coefficient perfect reconstruction QMF bank using CORDIC algorithms," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 6, pp. 1254–1265, Jun. 2006. DOI: 10.1109/TCSI.2006.870478.

[201] S.-C. Pei, Y.-D. Huang, S.-H. Lin, and J.-J. Shyu, "Design of variable comb filter using FIR variable fractional delay element," *Signal Processing*, vol. 92, no. 10, pp. 2409–2421, Oct. 2012. DOI: http://dx.doi.org/10.1016/j.sigpro.2012.03.001.

[202] S.-C. Pei, J.-J. Shyu, C.-H. Chan, and Y.-D. Huang, "An improved method for the design of variable fractional-delay IIR digital filters," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 05 15–18, Rio de Janeiro, Brazil, May 15–18, 2011, pp. 394–397. DOI: 10.1109/ISCAS.2011.5937585.

[203] S.-C. Pei, J.-J. Shyu, Y.-D. Huang, and C.-H. Chan, "Improved methods for the design of variable fractional-delay IIR digital filters," *IEEE Trans. Circuits Syst. I*, vol. 59, no. 5, pp. 989–1000, Apr. 2012. DOI: 10.1109/TCSI.2012.2188945.

[204] P. Persson, "EDDA — An algorithm for interactive design of hardware-efficient FIR filters," in *Proc. 2004 Swedish System-on-Chip Conference (SSoCC'04)*, Båstad, Sweden, Apr. 2004.

[205] P. Persson, S. Nordebo, and I. Claesson, "A multimode mean field annealing technique to design recursive digital filters," *IEEE Trans. Circuits Syst. II*, vol. 48, pp. 1151–1154, Dec. 2001. DOI: 10.1109/82.988942.

[206] —, "Design of digital filters with general hardware constraints by mean field annealing," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 2, Sydney, Australia, May 6–9, 2001, pp. 565–568. DOI: 10.1109/ISCAS.2001.921133.

[207] —, "Design of discrete coefficient FIR filters by a fast entropy-directed deterministic annealing algorithm," *IEEE Trans. Signal Processing*, vol. 53, no. 3, pp. 1006–1014, Mar. 2005. DOI: 10.1109/TSP.2004.842178.

[208] D. Petrov, A. Oborina, L. Giupponi, and T. H. Stitz, "Link performance model for filter bank based multicarrier systems," *EURASIP Journal on Advances in Signal Processing*, vol. 2014, no. 169, 2014. DOI: 10.1186/1687-6180-2014-169.

[209] P. Pracný, I. H. H. Jørgensen, and E. Bruun, "Interpolating by a factor of 3 in low-voltage low-power $\Sigma\Delta$ dac," *Analog Integrated Circuits and Signal Processing*, 2014. DOI: DOI10.1007/s10470-014-0327-8.

[210] —, "System-level optimization of a DAC for hearing-aid audio class D output stage," in *Technological Innovation for the Internet of Things*, L. M. Camarinha-Matos, S. Tomic, and P. Graça, Eds., vol. 394, ser. IFIP Advances in Information and Communication Technology, Springer Berlin Heidelberg, 2013, pp. 647–654. DOI: 10.1007/978-3-642-37291-9_70.

[211] M. F. Quélhas, "Projeto de filtros IIR por mapeamento de pólos e zeros," PhD thesis, Universidade Federal de Rio de Janeiro, Brazil, 2010. [Online]. Available: www.pee.ufrj.br/teses/textocompleto/2010080601.pdf.

[212] M. F. Quelhas and A. Petraglia, "Digital filter design optimization using partial cost functions," in *Proc. IEEE Int. Symp. Circuits Syst.*, Taipei, Taiwan, May 24–27, 2009, pp. 285–288. DOI: 10.1109/ISCAS.2009.5117741.

[213] M. F. Quélhas, A. Petraglia, and M. R. Petraglia, "Design of IIR filters using a pole-zero mapping approach," *Digit. Signal Process.*, vol. 23, no. 4, pp. 1314–1321, 2013. DOI: 10.1016/j.dsp.2013.03.007.

[214] M. F. Quelhas, A. Petraglia, and M. R. Petraglia, "Linear programming for the design of IIR filters," in *IEEE Third Latin American Symp. on Circuits and Syst.*, Quintana Roo, México, Feb. 29–Mar. 2, 2012, pp. 1–4.

[215] G. Ramirez-Conejo, J. Diaz-Carmona, J. G. Delgado-Frias, G. Jovanovic-Dolecek, and J. Prado-Olivarez, "Adjustable fractional delay FIR filters design using multirate and frequency optimization techniques," in *IEEE Convención de Centroamérica y Panamá, Trigésima Edición*, San José, Costa Rica, Nov. 17–19, 2010. [Online]. Available: http://b-dig.iie.org.mx/BibDig/P10-0961/nicaragua/C26.pdf.

[216] G. Ramirez-Conejo, J. Diaz-Carmona, A. Ramirez-Agundis, A. Padilla-Medina, and J. Delgado-Frias, "FPGA implementation of adjustable wideband fractional delay FIR filters," in *Int. Conf. Reconfigurable Computing and FPGAs*, Cancun, Mexico, Dec. 13–15, 2010, pp. 406–411. DOI: 10.1109/ReConFig.2010.68.

[217] M. Rautiainen and J. Malmivuo, "Iterative method for creating wavelet dictionaries," in *Proc. XI European Signal Processing Conf.*, vol. II, Toulouse, France, Sep. 3–6, 2002, pp. 591–594. [Online]. Available: http://www.eurasip.org/Proceedings/Eusipco/2002/articles/paper004.pdf.

[218] T. Rissa, R. Uusikartano, and J. Niittylahti, "Adaptive FIR filter architectures for run-time reconfigurable FPGAs," in *Proc. IEEE Int. Conf. Field-Programmable Technology*, 2002, pp. 52–59.

[219] D. E. T. Romero, M. G. Cruz Jimenez, and G. Jovanovic Dolecek, "Design of FIR Hilbert transformers using a combined frequency response masking/frequency transformation approach," in *Proc. Int. Midwest Symp. Circuits Syst.*, Boise, IL, USA, 2012, pp. 960–963. DOI: 10.1109/MWSCAS.2012.6292181.

[220] D. E. T. Romero and G. J. Dolecek, "Digital FIR hilbert transformers: fundamentals and efficient design methods," in *MATLAB – A Fundamental Tool for Scientific Computing and Engineering Applications*, V. N. Katsikis, Ed., InTech, 2012, pp. 445–482, ISBN: 978-953-51-0750-7. [Online]. Available: http://cdn.intechopen.com/pdfs/39362/InTech-Digital_fir_hilbert_transformers_fundamentals_and_efficient_design_methods.pdf.

[221] S. A. Samad, A. Hussain, and D. Isa, "Wave digital filters with minimum multiplier for discrete Hilbert transformer realization," *Signal Processing*, vol. 86, no. 12, pp. 3761–3768, Dec. 2006. DOI: 10.1016/j.sigpro.2006.03.005.

[222] R. Setiawan, V. P. Lesmana, and B.-H. Gwee, "Design and implementation of a low power FIR filter bank," *Journal of The Institution of Engineers, Singapore*, vol. 45, no. 5, pp. 77–87, 2005. [Online]. Available: http://www.ies.org.sg/journal/current/v45i5/v45i5_6.pdf.

[223] A. Shahein, Q. Zhang, N. Lotze, and Y. Manoli, "A novel hybrid monotonic local search algorithm for FIR filter coefficients optimization," *IEEE Trans. Circuits Syst. I*, 2012, to appear. DOI: 10.1109/TCSI.2011.2165409.

[224] Z. U. Sheikh, "Efficient realizations of wide-band and reconfigurable FIR systems," PhD thesis, Linköping Univ., Dept. Elect. Eng., Sweden, 2012.

[225] Z. U. Sheikh and H. Johansson, "A technique for efficient realization of wide-band FIR LTI systems," *IEEE Trans. Signal Processing*, vol. 60, no. 3, pp. 1482–1486, 2012. DOI: 10.1109/TSP.2011.2178408.

[226] —, "Efficient wide-band FIR LTI systems derived via multirate techniques and sparse bandpass filters," *IEEE Trans. Signal Processing*, vol. 60, no. 7, pp. 3859–3863, Jul. 2012. DOI: 10.1109/TSP.2012.2194712.

[227] T. Shen and Y. C. Lim, "Recursive digital filter design based on FRM approach," in *2010 Asia Pacific Conf. on Postgraduate Research in Microelectronics and Electronics*, Shanghai, China, Sep. 22–24, 2010, pp. 217–220. DOI: 10.1109/PRIMEASIA.2010.5604923.

[228] D. Shi and Y. J. Yu, "Design of discrete-valued linear phase FIR filters in cascade form," *IEEE Trans. Circuits Syst. I*, vol. 58, no. 7, pp. 1627–1636, 2011. DOI: 10.1109/TCSI.2011.2143250.

[229] —, "Design of linear phase FIR filters with high probability of achieving minimum number of adders," *IEEE Trans. Circuits Syst. I*, vol. 58, no. 1, pp. 126–136, 2011. DOI: 10.1109/TCSI.2010.2055290.

[230] V. Shuvaev, "Development of the methods of synthesis and the study of the characteristics of the low-sensitivity digital filters," PhD thesis, Krasnoyarsk, Khakassia Technological Institute, 2003. [Online]. Available: http://www.dissercat.com/content/sintez-chastotno-razdelitelnykh-i-soglasuyushchikh-tsepei.

[231] J.-J. Shyu and S.-C. Pei, "Minimax phase error design of allpass variable fractional-delay digital filters by iterative weighted least-squares method," *Signal Processing*, vol. 89, no. 9, pp. 1774–1781, 2009. DOI: 10.1016/j.sigpro.2009.03.021.

[232] J.-J. Shyu, S.-C. Pei, C.-H. Chan, Y.-D. Huang, and S.-H. Lin, "A new criterion for the design of variable fractional-delay FIR digital filters," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 2, pp. 368–377, Feb. 2010. DOI: 10.1109/TCSI.2009.2023835.

[233] E. A. B. da Silva, L. Lovisolo, A. J. S. Dutra, and P. S. R. Diniz, "FIR filter design based on successive approximation of vectors," *IEEE Trans. Signal Processing*, vol. 62, no. 15, pp. 3833–3848, Jul. 2014. DOI: 10.1109/TSP.2014.2324992.

[234] S. A. Skogstad, S. Holm, and M. Høvin, "Designing digital IIR lowpass differentiators with multi-objective optimization," in *IEEE 11th Int. Conf. Signal Process.*, vol. 1, Beijing, China, 2012, pp. 10–15. DOI: 10.1109/ICoSP.2012.6491617.

[235] S. A. Skogstad, S. Holm, and M. E. Høvin, "Digital IIR filters with minimal group delay for real-time applications," in *Int. Conf. Engineering and Technology*, Cairo, 2012, pp. 1–6. DOI: 10.1109/ICEngTechnol.2012.6396136.

[236] C. F. T. Soares, A. C. de Mesquita Filho, and A. Petraglia, "Optimizing capacitance ratio assignment for low-sensitivity SC filter implementation," *IEEE Trans. on Evolutionary Computation*, vol. 14, no. 3, pp. 375–380, Jun. 2010. DOI: 10.1109/TEVC.2009.2025033.

[237] —, "Using a genetic algorithm to optimize capacitance ratio approximations in SC filters," *Circuits, Syst., Signal Process.*, vol. 29, no. 4, pp. 687–707, 2010. DOI: 10.1007/s00034-010-9176-6.

[238] W. Sootkaneung, "The design of bit-serial lattice wave digital filter using FPGA," in *Fifth Int. Conf. Inform., Commun. and Signal Process.*, Dec. 6–9, 2005, pp. 559–563. DOI: 10.1109/ICICS.2005.1689109.

[239] G. K. Stoyanov, K. Nikolova, and M. Kawamata, "Low-sensitivity design of allpass based fractional delay digital filters," in *Digital Filters*, F. P. G. Márquez, Ed., Intech, Apr. 2011, ch. 7, pp. 155–178. [Online]. Available: http://www.intechopen.com/articles/show/title/low-sensitivity-design-of-allpass-based-fractional-delay-digital-filters.

[240] G. K. Stoyanov, K. S. Nikolova, and V. I. Markova, "High accuracy design and realization of fixed and variable allpass-based fractional delay digital filters," in *Int. Conf. Telecommun. in Modern Satellite, Cable, and Broadcasting Services (TELSIKS)*, Nis, Serbia, Oct. 7–9, 2009, pp. 167–176. DOI: 10.1109/TELSKS.2009.5339430.

[241] G. K. Stoyanov, Z. Nikolova, K. S. Ivanova, and V. I. Anzova, "Design and realization of efficient IIR digital filter structures based on sensitivity minimizations," in *Proc. IEEE Int. Conf. on Telecommun. in Modern Satellite, Cable and Broadcasting Services*, Serbia, Niš, Sep. 26–28, 2007, pp. 299–308. DOI: 10.1109/TELSKS.2007.4375998.

[242] A Torre Fernández, "Reception of wideband signals from geostationary collocated satellites with antenna arrays," *IET Communications*, vol. 8, no. 13, pp. 2229–2237, Sep. 2014.

[243] C.-C. Tseng, "Design of fractional delay filter using hermite interpolation method," *IEEE Trans. Circuits Syst. I*, vol. 59, no. 7, pp. 1458–1471, Jul. 2012. DOI: 10.1109/TCSI.2011.2177136.

[244] C.-C. Tseng and S.-L. Lee, "Design of wideband fractional delay filters using derivative sampling method," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 8, pp. 2087–2098, Aug. 2010. DOI: 10.1109/TCSI.2009.2037451.

[245] —, "Efficient design and implementation of variable fractional delay filters using differentiators," *IEEE Trans. Circuits Syst. I*, vol. 58, no. 6, pp. 1311–1322, Jun. 2011. DOI: 10.1109/TCSI.2010.2103157.

[246] M. Vasileios, "FIR filters of fixed coefficients," Master's thesis, Dept. Physics, Univ. Patras, Greece, 2008. [Online]. Available: http://nemertes.lis.upatras.gr/dspace/handle/123456789/1247.

[247] C.-Y. Wang, "Design and implementation of variable fractional-delay digital filters," Master's thesis, Dept. Electr. Eng., National University of Kaohsiung, Taiwan, 2010.

[248] C. Wang and H. K. Kwan, "Design of discrete coefficient frequency-response-masking FIR digital filters," in *Proc. IEEE Asia Pacific Conf. Circuits and Syst.*, 2008, pp. 461–464. DOI: 10.1109/APCCAS.2008.4746060.

[249] H. Wang, X. Cheng, P. Song, L. Yu, W. Hu, and L. Zhao, "An extrapolated impulse response filter design with sparse coefficients based on a novel linear approximation of matrix," *Circuits, Syst., Signal Process.*, 2014. DOI: 10.1007/s00034-014-9955-6.

[250] X.-H. Wang, Y.-G. He, and T.-Z. Li, "Neural network algorithm for designing FIR filters utilizing frequency-response masking technique," *J. Comput. Sci. Technol.*, vol. 24, no. 3, pp. 463–471, May 2009. DOI: 10.1007/s11390-009-9237-0.

[251] L. Wanhammar, B. Soltanian, K. Johansson, and O. Gustafsson, "Synthesis of circulator-tree wave digital filters," in *Proc. IEEE Conf. Image and Signal Process. Analysis*, Istanbul, Turkey, 2007, pp. 206–211. DOI: 10.1109/ISPA.2007.4383691.

[252] L. Wanhammar and Y. J. Yu, "Digital filter structures and their implementation," in *Academic Press Library in Signal Processing*, vol. 1, Elsevier Ltd., 2014, ch. 6, pp. 245–338.

[253] D. Wei, "Design of discrete-time filters for efficient implementation," PhD thesis, Dept. of Elect. Eng. and Computer Sci., Massachusetts Institute of Technology, USA, 2011. [Online]. Available: http://www.rle.mit.edu/dspg/documents/D.WeiPhDThesis.pdf.

[254] Y. Wei and D. Liu, "Improved design of frequency-response masking filters using band-edge shaping filter with non-periodical frequency response," *IEEE Trans. Signal Processing*, vol. 61, no. 13, pp. 3269–3278, Jul. 2013. DOI: 10.1109/TSP.2013.2259485.

[255] T. Wessoiiek, "Verfahren zum modulieren eines ersten basisband-signals und eines zweiten basisband-signals, modulator zur durchführung des verfahrens und verwendung des modulators in einer kabelkopfstelle," pat. DE102005024169, Nov. 2006.

[256] S. Wijaya, "Fixed-point realisation of erbium doped fibre amplifer control algorithms on FPGA," Master's thesis, School of Electrical, Electronic, and Computer Eng., University of Western Australia, Australia, 2008. [Online]. Available: https://repository.uwa.edu.au/R/-?func=dbin-jump-full&object_id=3840&local_base=GEN01-INS01.

[257] S. Wijaya and A. Cantoni, "A java simulation tool for fixed-point system design," in *Proc. 2nd Int. Conf. on Simulation Tools and Techniques*, Rome, Italy, Mar. 2–6, 2009. DOI: 10.4108/ICST.SIMUTOOLS2009.5606.

[258] J. Wu and S. Fengchun, "Design and application of a fractional delay compensation algorithm," *Astronomical Research & Technology*, vol. 8, no. 4, pp. 388–394, Oct. 2011.

[259] T. Xinguang, G. Lizhi, S. Chunlai, and Z. Eryang, "Optimal design of non-frequency-selective FIR digital filters based on windowing method," *J. Data Acquisition and Process.*, vol. 23, no. 2, pp. 228–232, Mar. 2008. [Online]. Available: http://ylikaaki.homenet.org/publications/EUSIPCO00/Xinguang08.pdf.

[260] F. Xu, C.-H. Chang, and C.-C. Jong, "A new integrated approach to the design of low-complexity FIR filters," in *Proc. IEEE Int. Symp. Circuits Syst.*, Island of Kos, Greece, May 21–24, 2006, pp. 601–604. DOI: 10.1109/ISCAS.2006.1692657.

[261] —, "Design of low-complexity FIR filters based on signed-powers-of-two coefficients with reusable common subexpressions," *IEEE Trans. Computer-Aided Design*, vol. 26, no. 10, pp. 1898–1907, Oct. 2007. DOI: 10.1109/TCAD.2007.895615.

[262] W. J. Xu, Y. J. Yu, and H. Johansson, "Improved filter bank approach for the design of variable bandedge and fractional delay filters," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 3, pp. 764–777, 2014. DOI: 10.1109/TCSI.2013.2284176.

[263] C. YANG, "Computationally efficient FIR digital filters," PhD thesis, Dept. of Elect. and Comput. Eng., National Univ. of Singapore, 2004. [Online]. Available: https://scholarbank.nus.edu/handle/10635/17082.

[264] C.-Y. Yao, W.-C. Hsia, and Y.-H. Ho, "Designing hardware-efficient fixed-point FIR filters in an expanding subexpression space," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 1, pp. 202–212, 2014. DOI: 10.1109/TCSI.2013.2268551.

[265] *A Polynomial-Time Algorithm for the Design of Multiplierless Linear-Phase FIR Filters with Low Hardware Cost*, Melbourne, Australia, 2014, pp. 970–973. DOI: 10.1109/ISCAS.2014.6865299.

[266] W. B. Ye and Y. J. Yu, "An algorithm for the design of low power linear phase FIR filters," in *Proc. Asia Pacific Conf. on Postgraduate Research in Microelectronics and Electronics*, Macao, China, Oct. 6–7, 2011, pp. 29–32. DOI: 10.1109/PrimeAsia.2011.6075063.

[267] —, "Bit-level multiplierless fir filter optimization incorporating sparse filter technique," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 11, pp. 3206–3215, 2014. DOI: 10.1109/TCSI.2014.2327287.

[268] —, "Design of high order and wide coefficient wordlength multiplierless FIR filters with low hardware cost using genetic algorithm," in *Proc. IEEE Int. Symp. Circuits Syst.*, Seoul, South Korea, 2012, pp. 45–48. DOI: 10.1109/ISCAS.2012.6272061.

[269] —, "Single-stage and cascade design of high order multiplierless linear phase FIR filters using genetic algorithm," *IEEE Trans. Circuits Syst. I*, vol. 60, no. 11, pp. 2987–2997, Nov. 2013. DOI: 10.1109/TCSI.2013.2256211.

[270] Z. Ye and C.-H. Chang, "A hybrid CSA tree for merged arithmetic architecture of FIR filter," in *Proc. 3th IEEE/EURASIP Int. Symp. on Image and Signal Processing and Analysis (ISPA-2003)*, Rome, Italy, Sep. 18–20, 2003, pp. 449–453. DOI: 10.1109/ISPA.2003.1296939.

[271] —, "Local search method for FIR filter coefficients synthesis," in *Proc. 2nd IEEE Int. Workshop on Electronic Design, Test, and Applications (DELTA-2004)*, Perth, Australia, Jan. 28–30, 2004, pp. 255–260. DOI: 10.1109/DELTA.2004.10042.

[272] K. S. Yeung, "The design and multiplier-less realization of a novel digital IF for software radio receivers," M. Phil. Thesis, The Univ. of Hong Kong, Aug. 2003. [Online]. Available: http://hub.hku.hk/bitstream/10722/30807/11/FullText.pdf.

[273] K. S. Yeung and S. C. Chan, "The design and multiplier-less realization of software radio receivers with reduced system delay," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 12, pp. 2444–2459, Dec. 2004. DOI: 10.1109/TCSI.2004.838253.

[274] C. Yu, K. L. Teo, and H. H. Dam, "Design of allpass variable fractional delay filter with signed powers-of-two coefficients," *Signal Processing*, vol. 95, pp. 32–42, 2014. DOI: 10.1016/j.sigpro.2013.08.005i.

[275] J. Yu, "Design and implementation of computationally efficient digital filters," PhD thesis, National Univ. of Singapore, 2005. [Online]. Available: http://scholarbank.nus.edu.sg/bitstream/handle/10635/17585/YuJH.pdf?sequence=1.

[276] J. Yu and Y. Lian, "Design equations for jointly optimized frequency-response masking filters," *Circuits, Syst., Signal Process.*, vol. 26, no. 1, pp. 27–42, Feb. 2007. DOI: 10.1007/s00034-005-0220-x.

[277] —, "Interpolation factor analysis for jointly optimized frequency-response masking filters," in *Proc. IEEE Int. Symp. Circuits Syst.*, Kobe, Japan, May 23–26, 2005, pp. 2016–1019. DOI: 10.1109/ISCAS.2005.1465012.

[278] Y. J. Yu and Y. C. Lim, "Optimization of linear phase FIR filters in dynamically expanding subexpression space," *Circuits, Syst., Signal Process.*, vol. 29, no. 1, pp. 65–80, Feb. 2010. DOI: 10.1007/s00034-009-9114-7.

[279] —, "Signed power-of-two allocation scheme for the design of lattice orthogonal filter banks," in *Proc. IEEE Int. Symp. Circuits Syst.*, Kobe, Japan, May 23–26, 2005, pp. 1819–1822. DOI: 10.1109/ISCAS.2005.1464963.

[280] Y. J. Yu, Y. C. Lim, and D. Shi, "Low complexity design of variable bandedge linear phase FIR filters with sharp transition band," *IEEE Trans. Signal Processing*, vol. 57, no. 4, pp. 1328–1338, Apr. 2009. DOI: 10.1109/TSP.2008.2010597.

[281] Y. J. Yu, T. Saramäki, and Y. C. Lim, "An iterative method for optimizing FIR filters synthesized using the two-stage frequency-response masking technique," in *Proc. IEEE Int. Symp. Circuits Syst.*, Bangkok, Thailand, May 25–28, 2003. DOI: 10.1109/ISCAS.2003.1205159.

[282] Y. J. Yu, D. Shi, and Y. C. Lim, "Design of extrapolated impulse response FIR filters with residual compensation in subexpression space," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 12, pp. 1328–1338, 2009. DOI: 10.1109/TCSI.2009.2016165.

[283] Y. J. Yu, K. L. Teo, Y. C. Lim, and G. H. Zhao, "Extrapolated impulse response filter and its application in the synthesis of digital filters using the frequency-response masking technique," *Signal Processing*, vol. 85, no. 3, pp. 581–590, Mar. 2005. DOI: 10.1016/j.sigpro.2004.11.03.

[284] Y. J. Yu and W. J. Xu, "Investigation on the optimization criteria for the design of variable fractional delay filters," *IEEE Trans. Circuits Syst. II*, vol. 60, no. 8, pp. 522–526, 2013. DOI: 10.1109/TCSII.2013.2268239.

[285] —, "Mixed-radix fast filter bank approach for the design of variable digital filters with simultaneously tunable bandedge and fractional delay," *IEEE Trans. Signal Processing*, vol. 60, no. 1, pp. 100–111, 2012, to appear. DOI: 10.1109/TSP.2011.2170169.

[286] M. Z. Zhang and V. K. Asari, "A design methodology for performance-resource optimization of a generalized 2D convolution architecture with quadrant symmetric kernels," in *Advances in Computer Systems Architecture*, vol. 4697/2007, ser. Lecture Notes in Computer Science, Springer Berlin / Heidelberg, 2007, pp. 220–234. DOI: 10.1007/978-3-540-74309-5_22.

[287] —, "An efficient multiplier-less architecture for 2-D convolution with quadrant symmetric kernels," *The VLSI Journal Integration*, vol. 40, no. 4, pp. 490–502, Jul. 2007. DOI: 10.1016/j.vlsi.2006.07.001.

[288] M. Z. Zhang, H. T. Ngo, and V. K. Asari, "Design of an efficient multiplier-less architecture for multi-dimensional convolution," in *Proc. 10th Asia-Pacific Conf. Advances in Comput. Syst. Arch.*, Singapore, Oct. 2005, pp. 65–78. DOI: 10.1007/11572961_7.

[289] —, "Multiplier-less VLSI architecture for real-time computation of multi-dimensional convolution," *Microprocess. Microsyst.*, vol. 31, no. 1, pp. 25–37, 2007. DOI: 10.1016/j.micpro.2006.07.004.

[290] M. Z. Zhang, M.-J. Seow, and V. K. Asari, "A hardware architecture for color image enhancement using a machine learning approach with adaptive parameterization," in *Int. Joint Conf. on Neural Networks*, Vancouver, BC, Canada, Jun. 16–21, 2006, pp. 35–40. DOI: 10.1109/IJCNN.2006.246656.

[291] —, "A high performance architecture for color image enhancement using a machine learning approach," *International Journal of Computational Intelligence Research (IJCIR)*, vol. 2, no. 1, pp. 40–47, 2006.

[292] M. Z. Zhang, M.-J. Seow, L. Tao, and V. K. Asari, "A tunable high-performance architecture for enhancement of stream video captured under non-uniform lighting conditions," *Microprocessors & Microsystems archive*, vol. 32, no. 7, pp. 386–393, Oct. 2008. DOI: 10.1016/j.micpro.2008.04.002.

[293] —, "Design of an efficient architecture for enhancement of stream video captured in non-uniform lighting conditions," in *Int. Symp. Signals, Circuits Syst.*, vol. 2, Jun. 13–14, 2007, pp. 1–4. DOI: 10.1109/ISSCS.2007.4292756.

[294] M. Z. Zhang, L. Tao, M.-J. Seow, and V. K. Asari, "Design of an efficient flexible architecture for color image enhancement," in *Advances in Computer Systems Architecture*, vol. 4186/2006, ser. Lecture Notes in Computer Science, Springer Berlin / Heidelberg, 2006, pp. 323–336. DOI: 10.1007/11859802_26.

[295] S. Zhang, J. Qi, and J. Bao, "The improvement of design for CIC compensation filter," in *2011 Int. Conf. Electronics, Communications and Control (ICECC)*, Ningbo, China, Sep. 9–11, 2011, pp. 1712–1715. DOI: 10.1109/ICECC.2011.6067850.

[296] Y. Zhang, "Design and realization of FIR and bireciprocal wave digital filters," Master's thesis, Dept. of Electr. and Comput. Eng., Univ. of Manitoba, Winnipeg, Manitoba, Canada, Apr. 2000. [Online]. Available: https://mspace.lib.umanitoba.ca/bitstream/1993/2412/1/MQ51826.pdf.

[297] Z. Q. Zhang, "Design and implementation of a multi-standard video format conversion interface circuit," Master's thesis, University of Electronic Science and Technology, China, 2006.

[298] H.-j. ZHAO, M. LI, M.-t. CUI, P. Bin, and L. Ming-dong, "Realization of linear phase recursive IIR digital filters based on optimal state variable," *Journal of Yunnan University*, vol. 36, no. 2, 193–198, 2014. DOI: 10.7540/j.ynu.20130082.

[299] H. Zhao, H. K. Kwan, L. Wan, and L. Nie, "Design of 1-D stable variable fractional delay IIR filters using finite impulse response fitting," in *IEEE Int. Conf. Commun., Circuits Syst.*, vol. 1, Guilin, China, 2006, pp. 201–205. DOI: 10.1109/ICCCAS.2006.284618.

[300] H. Zhao and J. Yu, "Design of 1-D variable fractional delay all-pass filters using stability controlling," in *Proc. Int. Conf. Commun., Circuits and Syst.,*, 2009, pp. 894–897. DOI: 10.1109/ICCCAS.2009.5250362.

[301] L. Zhou, W. Pei, P. Xi, and Z. He, "Extrapolated impulse response filter using coefficient-autocorrelation-matrix decomposition," *Signal Processing*, vol. 88, no. 7, pp. 1762–1774, 2008. DOI: 10.1016/j.sigpro.2008.01.014.