# *DESIGN AND REALIZATION OF CONTINUOUS-TIME WAVE DIGITAL FILTERS*

Dieter Brückmann
Faculty of Electrical, Information and Media Engineering
University of Wuppertal,
D-42119 Wuppertal, Germany
e-mail: brueckm@uni-wuppertal.de

**Abstract—Digital signal processing in continuous-time can result in a number of advantages compared to classical sampled data systems, while the inherent advantages of digital implementations with respect to programmability and noise immunity are retained. It turned out however that a critical point of these systems is the implementation of the continuous-time delays, requiring a considerably larger chip area than the delays in sampled data systems. Thus structures with a minimum number of delay elements seem to be advantageous. In this contribution the implementation of continuous-time wave digital filters (WDFs) is considered. This filter type is well-known for its superior properties with respect to stability and sensitivity. Furthermore, by selecting a proper reference structure, WDFs can be implemented with a minimum number of delay elements for a given filter specification thus making them very attractive for continuous-time implementations. Due to the proposed concept a number of advantages are obtained and a very efficient realization in VLSI-technology becomes feasible.**

## I. INTRODUCTION

Recently a new type of signal processing system has been proposed, which performs digital signal processing in the continuous time domain [1-3]. The respective signals are discrete in amplitude but continuous in time. Such systems, also called "CTDA-systems" in the literature [1], are clockless, thus asynchronous realizations [4] are a straight-forward way of implementation. Contrary to classical asynchronous implementations however, the time interval between the samples must be also preserved, since it carries information. Thus the delays cannot be implemented as simple binary storage elements, but must be realized as continuous time delay lines. Therefore the implementation of the delay elements in continuous time systems is a critical point with respect to the required chip area and the accuracy.

Despite this possible drawback digital continuous-time systems have a number of interesting properties, making them very attractive for a number of applications. Whereas the advantages of digital techniques, such as programmability and noise immunity still hold, no aliasing of out-of-band signals and quantization noise occurs due to the continuous-time signal processing.

Furthermore, since signal processing only has to be performed when signals are changing, such systems have the potential for implementations which are optimized for minimum power. In conventional digital systems the dominant dynamic power consumption is determined by the sampling frequency, which must be at least twice the bandwidth of the input signal. Thus the power consumption does not depend on the actual spectral content of the input signal. The dynamic power consumption of continuous-time digital systems however is directly proportional to the spectral content of the input signal.

In [1-3] it has been proposed to decompose the input signal $x(t)$ into N binary functions $x_i(t)$, which can take only the values 0 and 1. The binary input signals $x_i(t)$ can be seperately processed then by N simple continuous-time digital signal processors in parallel. The signal $x(t)$ is thus approximated by $x_a(t)$ given by:

$$x_a(t) = \sum_{i=1}^{N} 2^{-i} x_i(t)$$

The binary signals $x_i(t)$ are still continuous in time. Such signals can be generated by continuous-time analog-to-digital converters with no clock. The waveform of the input signal determines the time instants $t_i$ when the signals $x_i(t)$ are changing. The binary input signals are processed in the DSP-section by digital processors consisting of adders, multipliers and continuous-time delays. This digital decomposition of the input signal seem to be advantageous for continuous-time implementations, as has been shown in [1-3] for non-recursive systems. In the following this method will be also applied to recursive systems.

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## II. CONTINUOUS-TIME RECURSIVE DIGITAL FILTERS

The transfer function of a recursive filter of order n can be described by an $n^{th}$-order denominator polynomial and a numerator polynomial of order m≤n. In order to reduce the sensitivity with respect to coefficient quantization, the transfer function is factorized in second-order product terms and one first order term for odd order filters. Such a system can be implemented by a cascade connection of second-order blocks, and one first order block for odd-order filters. The transfer function H(s) of a continuous-time second order digital filter block is given in the frequency domain s by:

$$H(s) = \frac{B_0 + B_1 e^{-sT} + B_2 e^{-2sT}}{1 + A_1 e^{-sT} + A_2 e^{-2sT}}, \qquad (2)$$

where T is the fixed delay of one delay element D and the $B_i$'s and $A_i$'s are the filter coefficients. The frequency response is periodic with frequency $2\pi/T$ even though no aliasing occurs.

The Laplace transform Y(s) of the output signal y(t) of the filter block is obtained from the Laplace transform $X_a(s)$ of the input $x_a(t)$ according to

$$Y(s) = H(s) \cdot X_a(s) \cdot \qquad (3)$$

Using binary decomposition of $x_a(t)$ each binary bit-stream must be filtered by the transfer function according to eq. (2). Figure 1 shows the respective realization. Each of the N parallel filter blocks contains two binary delay elements.

Since the inputs to the multipliers are binary, the multipliers are degenerated to simple gating functions thus considerably simplifying the implementation. For an input signal of 1 the coefficient value is gated to the adders and for a zero no gating is performed. Thus the overall realization is significantly simplified by using N parallel filter block with the word-length of 1 Bit. The output signal y(t) is generated by a continuous-time adder array taking the binary weighting of the respective filter block outputs into account. A second adder array is required at the input of the filter blocks realizing the recursive functionality.

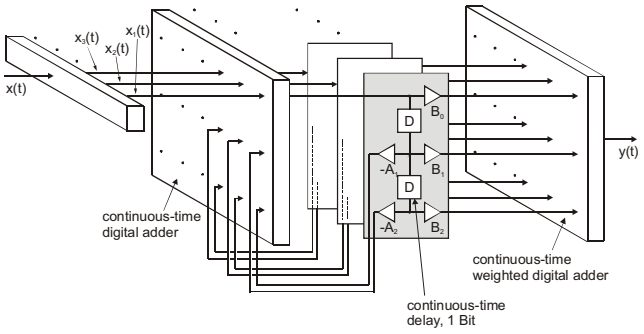


Figure 1. Decomposition of a recursive continuous-time digital filter block of order 2.

## III. CONTINUOUS-TIME WAVE DIGITAL FILTERS

Recursive filters based on wave digital filters [5-7] have a number of advantages compared to the structure considered up to now. Especially they have superior stability properties even under nonlinear operating conditions caused by rounding or overflow. Furthermore for a fixed word-length they have a better dynamic range than filters with cascaded general second order blocks. Wave digital filters are derived from a passive reference prototype and the superior properties of the analog reference structure are mapped to the digital filter when properly designed. For the realization of wave digital filters there exists a number of different structures. It turned out that wave digital filters in lattice structure [5-7], result in implementations with minimum hardware requirements. The coefficients of these filters can be easily obtained from explicit formulas as described in [6]. Respective software tools are available for the coefficient computation.

Lattice wave digital filters are composed of two branches which consist of cascaded second order allpass sections and one first order allpass in the upper branch as shown in fig. 2. Since the number of delay elements is canonical, these structures seem to be well-suited for continuous-time implementations.

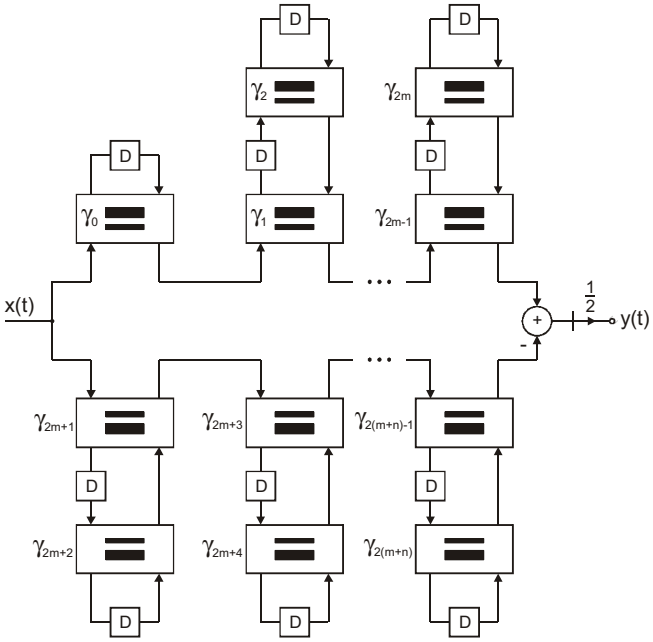


Figure 2. Continuous-time Wave Digital Filter in lattice structure.

The transfer function H(s) of this continuous-time wave digital filter can be described by the transfer functions $H_1(s)$ and $H_2(s)$ of the two allpass branches:

$$H(s) = \frac{H_1(s) - H_2(s)}{2} \tag{4}$$

For the transfer function $A_1(s)$ of the continuous-time first order allpass section holds:

$$A_1(s) = \frac{-\gamma_0 + e^{-sT}}{1 - \gamma_0 \cdot e^{-sT}} \tag{5}$$

where the coefficient $\gamma_0$ is in the range $-1<\gamma_0<+1$. By comparing this expression with eq. (2) a respective implementation according to fig. 1 is obtained with $B_2=A_2=0$, $B_0=A_1=-\gamma_0$ and $B_1=1$, as shown in fig. 3a.
For the second order sections with coefficients $\gamma_1$ and $\gamma_2$ following equation holds respectively:

$$A_2(s) = \frac{-\gamma_1 + \gamma_2 \cdot (\gamma_1 - 1) \cdot e^{-sT} + e^{-2sT}}{1 + \gamma_2 \cdot (\gamma_1 - 1) \cdot e^{-sT} - \gamma_1 \cdot e^{-2sT}} \tag{6}$$

Comparing this expression also with eq. (2) the respective coefficients are given by $B_0=A_2=-\gamma_1$, $B_1=A_1=\gamma_2\cdot(\gamma_1-1)$ and $B_2=1$. The respective realization is shown by fig. 3b. Further savings can be obtained by using bireciprocal wave digital filters for implementation [6-9]. This filter type can be used if the filter transfer function is approximately symmetrical to ¼ of the sampling frequency. For continuous-time WDFs this corresponds to a symmetry with respect to $2\pi/T$, where T is the fixed delay of each delay element.
Bireciprocal lattice wave digital filters are a special case of lattice WDFs and can be implemented very efficiently, since 50% of the filter coefficients are zero and thus must not be realized. The respective transfer function of the 2nd-order allpass sections is given by:

$$A_1(s) = \frac{-\gamma_1 + e^{-2sT}}{1 - \gamma_1 \cdot e^{-2sT}} \tag{7}$$

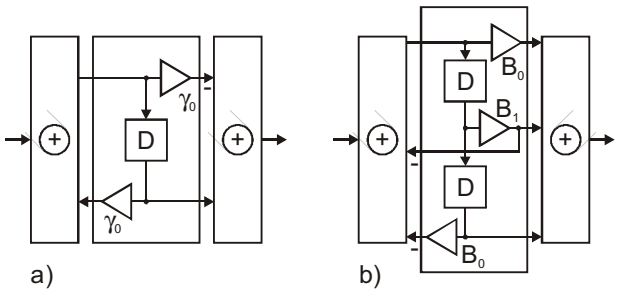


Figure 3. Realization of 1st-order (a) and 2nd-order (b) allpass sections.

For realization the structure in fig. 3a can be used with delays of D=2T. The 1st-order section degenerates to a pure delay with D=T.

## IV. DESIGN AND OPTMIZATION OF A CONTINUOUS-TIME LOWPASS WDF

In the following the design and implementation of a continuous-time lowpass filter will be considered. In order to have a reference for implementation costs the filter specification given in [1] was used. The passband and stopband edge frequencies are 3.4kHz and 4.6kHz respectively for a minimum stopband attenuation of 60dB. The unit delay was chosen to 62.5µs corresponding to a repetition frequency for the transfer characteristic of 16kHz. The input signal was quantized to 12 Bits. The design process described in [1] resulted in an FIR filter of order 28, where a large passband ripple of 1dB however was tolerated.

It turned out that either a lattice wave digital filter of order 7 or two cascaded bireciprocal WDFs of orders 5 each, fulfill the specification. The optimized coefficient values of the 2 wave digital filters are listed in table I.

TABLE I: OPTIMIZED WAVE DIGITAL FILTER COEFFICIENTS.

| Lattice WDF 7th-order | Bireciprocal Lattice WDF 2x 5th-order |
|---|---|
| $\gamma_0 = 2^{-1}-2^{-4}$ | $\gamma_{11}=2^{-2}+2^{-5}$ |
| $B_{10}= 2^{-1}-2^{-3}-2^{-5}$ | $\gamma_{12}=-1+2^{-2}$ |
| $B_{11}=-1+2^{-2}+2^{-6}$ | $\gamma_{21}=2^{-2}$ |
| $B_{20}= 2^{-1}+2^{-3}-2^{-7}$ | $\gamma_{22}=-1+2^{-2}$ |
| $B_{21}=-2^{-1}+2^{-4}-2^{-6}$ | |
| $B_{30}= 1-2^{-3}-2^{-6}$ | |
| $B_{31}=-2^{-1}+2^{-3}+2^{-5}$ | |

In a conventional design the cascaded bireciprocal filters result in the optimum solution with respect to implementation costs due to the simple coefficients and the reduced number of adders required [7-9]. However the increased number of delay elements, which is 10 compared to 7 for the 7th-order lattice filter, could be a severe drawback for a continuous-time design.

Both filters had been optimized for a signal-to-noise ratio of 60dB. Whereas the 7th-order lattice filters requires a wordlength of 14 Bits for the delay elements, this is reduced to 10 Bits for the 1st stage of the bireciprocal filter. The 2nd stage also requires a wordlength of 14 Bits. The frequency characteristics of the three filters generated with simulation models based on MATLAB/SIMULINK are shown in fig. 4.
The WDFs are designed for a passband ripple 0.1dB, which seems to be a more appropriate value for most applications compared to the 1dB of the FIR-Filter in [1].
Figure 4 shows the frequency response from 0 to 16 kHz, which is symmetric to 8 kHz due to the periodicity with 1/T=16kHz. Even though the frequency response is periodic, no aliasing occurs due to the continuous-time operation of the filter.

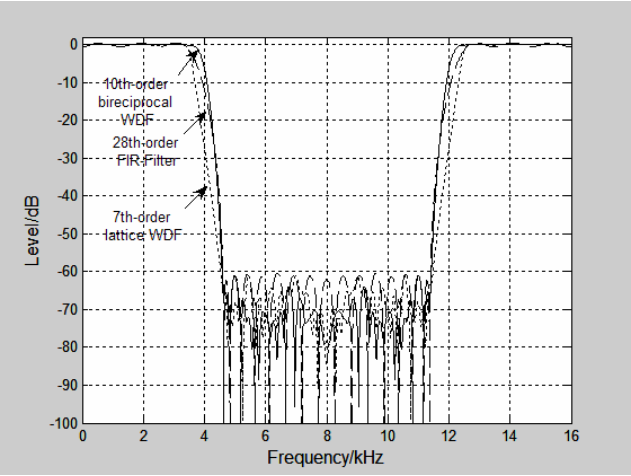


Figure 4. Frequency characteristics of the continuous-time filters with optimized coefficient values and minimum internal wordlength.

In order to compare the different realizations with respect to implementation costs following cost function was defined:

$$CO = \sum_{n=1}^{N} m_{0,n} + \sum_{i=1}^{(L-1)/2} \sum_{n=1}^{N} m_{i,n} + F \cdot \sum_{i=1}^{L} \sum_{n=1}^{N} d_{i,n}, \qquad (8)$$

where N is the required wordlength and corresponds to the number of parallel processing blocks in fig. 1. L is the filter order, $m_{i,n}$ is the number of 1-Bit adders in section i, and $d_{i,n}$ is the number of 1-Bit delay elements in the respective section. The number of adders in each first order section is given by $m_{0,n}$. The form factor F is determined by the ratio of the chip area required for a 1-Bit delay element to the chip area for a 1-Bit adder.

Taking the coefficient representation according to table I into account, 574 adders (1-Bit) and 98 delay elements (1- Bit) are required for the 7th-order lattice filter. The 10th-order bireciprocal filter can be realized with 194 adders and 120 delay elements. Thus, using eq. 8, it turns out that for form factors F greater than 17 the 7th-order filter is the better solution with respect to implementation costs, otherwise the bireciprocal filter is the WDF-architecture to be preferred.

A direct implementation of the FIR-filter requires 28x12=336 delay elements and more than 300 adders, which results in drastically increased implementation costs compared to the recursive filter structures.

The granularity required for the continuous-time delay elements is determined by the highest rate of change of the input signal. This granularity is directly related to the chip area required for implementation.

In [1] and [2] an architecture with an ADC using delta modulation was proposed, so that the input signal to the FIR-Filter is represented by a 1-Bit stream. Thus 1-Bit delay elements for each tap are sufficient and a 1-Bit signal representation can be used for most of the datapath.

Thus the required chip area can be reduced for the FIR-Filter. Due to the recursive structure this does not hold however for the delay elements of the WDFs, if the wordlength of the input signal is 1 Bit.

## V. Conclusions

Continuous-time digital filters, recently proposed, can have some advantages compared to conventional sampled data systems. Due to the nonsampled operation no aliasing of higher frequency components and of noise occurs and due to the asynchronous operation the power consumption can be minimized.

In this contribution it had been shown how to implement recursive continuous-time filters. In order to compare the implementation costs of different filter architectures a cost function had been defined. Using this cost function two different structures of wave digital filters had been compared to each other and to a continuous-time FIR-filter. It turned out that it can be advantageous with respect to implementation costs to use the recursive filter structures. It has been shown that the required chip area can be considerably reduced if the filter is properly designed.

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