FILTER STAGES FOR A HIGH-PERFORMANACE RECONFIGURABLE RADIO RECEIVER WITH MINIMUM SYSTEM DELAY

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ABSTRACT

In order to cope with the requirements of future mobile systems, there is a growing interest in the use of flexible but also highly optimized digital signal processing in mobile systems. In this contribution a novel solution for the realization of the digital signal processing for multimode-, multi-band-, and multifunctional wireless systems will be presented. It will be shown that a superior performance compared to state-of-the-art software defined radios can be obtained by using the proposed architecture. Main functional blocks are a special class of wave digital filters for sample rate conversion with integer values and an adjustable fractional delay filter. Thus also fractional decimation ratios can be realized enabling full flexibility. The design and optimization of these filters will be described in detail.
Due to the proposed concept a number of advantages are obtained and a very efficient realization in VLSI-technology becomes feasible. The concept has been confirmed by an implementation on an FPGA.

Index Terms— Reconfigurable Receiver, Wave digital filters, variable delay filter, fractional delay filter

1. INTRODUCTION

Recently a variety of architectures for software radio platforms have been presented in the literature [1-3]. These architectures are designed to make mobile systems more flexible. Most of them are however not well-suited for future mobile terminals since they do not take restrictions with respect to low costs, low power consumption, and small size into account. Therefore in this contribution a flexible but also highly optimized receiver concept will be proposed, which accounts for all of these different requirements.
Flexibility with respect to the bandwidth requirements of different mobile standards can be obtained by performing channel selection in the digital domain, where it can be implemented by programmable digital filters. The A/D-converter in such a concept digitizes the wideband input signal, containing the desired channel together with the unwanted adjacent channel interferers. Very attractive solutions are obtained when using ΣΔ-modulators with over-sampling for the digitization. In such a concept no additional filtering for channel selection is required since the adjacent channel interferers are suppressed by the decimation stages together with the high-pass shaped quantisation noise. Furthermore the requirements to the anti-aliasing low-pass filter are reduced due to over-sampling.

To account for low costs and low power the decimation filters must be optimized for an FPGA- or ASIC-implementation [2-4]. Thus the number of multiplications and MAC-operations should be kept to a minimum. Furthermore the decimation ratio of the filters should be adjustable so that the required flexibility with respect to the bandwidth and/or dynamic range is obtained. In order to allow the implementation of a fast AGC, which reduces the dynamic range requirements to the ADC, the group delay of the filters should be minimum. Finally no significant group delay distortion may be introduced in the pass-band.
Different types of filter structures for the decimation stages have been proposed in the literature [1-3]. None of them however fulfills the above mentioned requirements completely. Therefore in this contribution novel decimation filters will be proposed, which better fit to the above requirements. It will be shown that a special class of lattice wave digital filters in combination with an adjustable delay filter are very well suited for such a flexible concept.

2. DIGITAL SIGNAL PROCESSING STAGES

Fig. 1 shows the block diagram with the digital filter stages of the receiver path. Before decimation the quadrature down conversion of the received broadband signal to a low IF is performed in the analogue domain. The I and Q components of the IF-signal are digitized by A/D-converters then and down-converted to base-band by a complex digital mixer.
Sample rate reduction and channel-selection is then performed by the decimation filters, together with the suppression of the quantisation noise. It is well-known that the hardware required for the decimation filters can be minimized by performing decimation in several stages, with

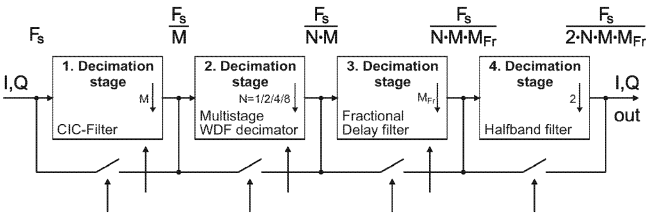

Fig. 1: Decimation filters in the receive path.

sample rate reduction after each stage, as shown in fig. 1. The first filter stage performs decimation by a programmable factor M. Since this filter is running at the highest clock frequency it should be implemented by rather simple filter structures. Thus cascaded integrator-comb (CIC) filters are used, which can be implemented by using only registers and adders.

For the lower decimation stages filters with a steeper transition band are needed. Very hardware efficient realizations are obtained by using optimized bireciprcal wave digital filters with approximately linear phase [5, 6]. The 2nd decimation stage consists of 3 cascaded WDFs, each of them performs a decimation by a factor of 2 and can be bypassed if required. Thus the decimation ratio N of the 2nd stage can be adjusted to 1, 2, 4, or 8. The 3rd decimation stage realizes the fractional decimation ratio M_{Fr} which can be programmed in the range of 1 to 2. The design of this stage is described in chp. 4 in more detail. The requirements to this filter are relaxed due to the 4th decimation stage which reduces the sampling rate further by a factor of 2. This filter can be also implemented as a bireciprocal WDF. However the requirements with respect to a linear phase are more severe for this filter than for the other stages. This requirement can be fulfilled with an additional low-order group delay equalizer to be cascaded with this stage.

The overall decimation ratio is programmable in a wide range (4-1000) since each decimation stage can be bypassed, and due to the adjustable values. The filters are designed for a stop-band attenuation of 100 dB with a pass-band ripple of 0.01 dB. Thus the requirements of nowadays mobile and wireless standards can be fulfilled. Typical sampling rates for A/D-converters used in state-of-the art software defined radios are in the range of 160 Mbit/s. Looking at GSM, the base-band bit-rate is 270 kbit/s, thus a decimation ratio of 590,77 must be realized for this typical application. The respective values to be adjusted are M=32, N=8 and M_{Fr}=1.15.

3. WAVE DIGITAL FILTER STAGES

The lower decimation stages can be very efficiently implemented by cascaded low-order bireciprocal lattice wave digital filters. Bireciprocal lattice wave digital filters are a special case of lattice WDFs and have a symmetrical filter characteristic with respect to ¼ of the sampling frequency [7]. The transfer function of N cascaded bireciprocal lattice wave digital filters is given by following relationship:

$$H(z) = 2^{-N} \prod_{i=i}^{N} [H_{i0}(z^2) + z^{-1} H_{i1}(z^2)] \ , \qquad (1)$$

where $H_{i0}(z)$ and $H_{i1}(z)$ are all-pass transfer functions. Using this cascade connection of low order WDFs results in a number of advantages compared to other solutions [5,6,8].

At first the realization costs are low since the number of coefficients to be implemented is reduced by 50% and the filter can run with the lower sampling frequency. By cascading low-order sections a high stop-band attenuation can be obtained with low coefficient sensitivity. Thus the optimized coefficients can be represented by very simple values and a wordlength of only a few bits is required. Due to the very simple coefficient representation, no general multiplier is needed, thus minimizing the implementation costs again. Furthermore the shorter wordlength also holds for the signal representation, resulting in reduced implementation costs for the adders and registers. Since the cascaded low-order sections are very modular, they are well suited for VLSI-implementation.

The orders and the coefficient values of the 4 wave digital filters designed for the decimation stages of the receiver are listed in table I. All coefficients are optimized and can be represented by a maximum of two shift-and-add operations. The attenuation characteristics of the filters are shown in fig. 2. A minimum stop-band attenuation of 100 dB is achieved.

Stage 2 WDF 1	Stage 2 WDF 2	Stage 2 WDF 3	Stage 4 WDF 4
2x3rd-order	2x3rd-order	2x5th-order	2x7th-order
$\gamma=2^{-1}-2^{-3}-2^{-5}$	$\gamma=-2^{-3}-2^{-5}-2^{-7}$	$\gamma_1=2^{-3}+2^{-5}+2^{-7}$	$\gamma_1=2^{-3}-2^{-7}$
----	----	$\gamma_2=-2^{-2}+2^{-3}$	$\gamma_2=2^{-1}-2^{-4}+2^{-8}$
----	----	----	$\gamma_3=2^{-2}-2^{-4}+2^{-6}$

Table I: Optimized wave digital filter coefficients.

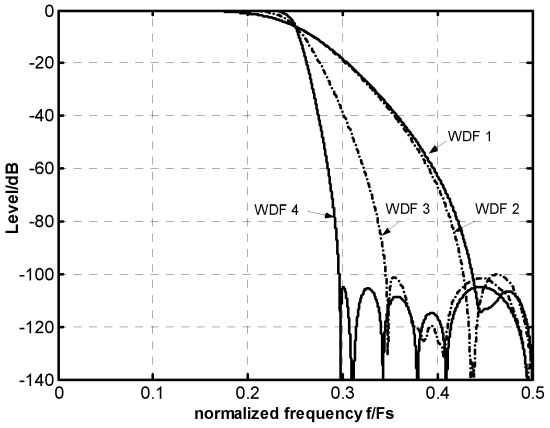

Fig. 2: Frequency characteristics of the wave digital filter stages performing each a decimation by 2.

4. FRACTIONAL DELAY FILTER

In order to adjust the fractional down-sampling ratios a variable digital filter is required. A very efficient method for the implementation in a reconfigurable receiver is to use an adjustable fractional delay FIR filter behind the integer decimators [3]. The proposed sample rate converter is designed such that this filter has to realize a down-sampling ratio between 1 and 2. Thus an expensive programmable FIR filter, used in classical sample rate converters [1-3], can be avoided. The parameter Φ, which must be adjusted with every new input value, can be determined from the down-sampling ratio M_{Fr} by following relationship:

$$\Phi(k) = floor[k \cdot M_{Fr}] - 0.5, \quad k = 0,1,2,3,.. \qquad (2)$$

A simple and efficient design method for adjustable fractional delay filters was proposed in [9] and will be applied in the following. The resulting variable filter can be implemented with the well-known Farrow-structure [10]. We will use however a modified version of the Farrow structure, where the sub-filters $H_k(z)$ can have different orders. The respective block diagram is shown in fig. 3. This results in a more efficient realization, as was outlined in [9]. The ideal frequency response of the adjustable delay filter is given by:

$$H_d^{\Phi}(e^{j\omega T}, \Phi) = e^{-j\omega\tau(\Phi)} \qquad (3)$$

where $\tau(\Phi)=D+\Phi$ is the group delay. Hereby D is an integer constant and the adjustable parameter Φ provides the arbitrary fractional delay. This function can be approximated by a Taylor series, which can be written as:

$$e^{-j\omega\tau(\Phi)} = e^{-j\omega D} \cdot \sum_{k=0}^{L} \frac{(-j\Phi\omega T)^k}{k!} + R \qquad (4)$$

The remainder R corresponds to the error when approximating the transfer function by L Taylor coefficients. For R holds:

$$|R| \le \frac{(-j\Phi\omega T)^{L+1}}{(L+1)!} \quad \forall\Phi, \forall\omega T, \forall L \qquad (5)$$

A straightforward realization of the expression above is obtained by the Farrow structure, where each Taylor coefficient is approximated by one sub-filter. Since the coefficient for k=0 is a constant, one of the sub-filters is degenerated to a pure delay. The multiplication with Φ^k can be separated from the sub-filters, as shown in fig. 3. The transfer function $H_{FD}(z,\Phi)$ of the overall filter is given by:

$$H_{FD}(z,\Phi) = \sum_{k=0}^{L_{FD}} \left[\sum_{i=0}^{N-1} h_{k,i} \cdot z^{-i} \right] \cdot \Phi^k \qquad (6a)$$

$$= \sum_{k=0}^{L_{FD}} H_k(z) \cdot \Phi^k \qquad (6b)$$

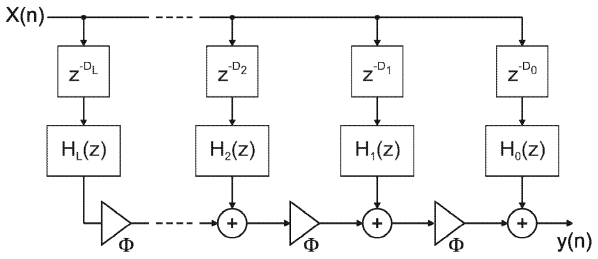

Fig. 3: Adjustable fractional delay FIR filter based on the Farrow structure.

where the $H_k(z)$ are the transfer functions of the sub-filters approximating the Taylor coefficients. The FIR-sub-filters in the L branches have fixed coefficients, which can be represented in CSD-code so that only shift-and-add operations have to be performed. Only the implementation of the multiplication with Φ requires a limited number of variable multipliers. The parameter Φ controls the phase delay of the filter.

Besides the realization of the fractional delay a down-converter stage also has to fulfill spectral requirements. In this stage the residual interference not suppressed by the integer decimators has to be attenuated. Thus the filter should be designed so that jointly the fractional delay requirements are fulfilled in the pass-band and the attenuation requirements are fulfilled in the stop-band. Taking these considerations into account, eq. (3) is modified as follows:

$$H_d^{\Phi}(e^{j\omega T}, \Phi) = \begin{cases} e^{-j\omega\tau(\Phi)} & 0 \le |\omega| \le \omega_p \\ 0 & \omega_s \le |\omega| \le \pi \end{cases} \qquad (7)$$

where ω_p and ω_s are the pass-band and the stop-band edge frequencies respectively.

5. DESIGN OF THE FRACTIONAL DELAY FILTER

Based on these formulas a suitable filter for the sample rate converter in fig. 1 has been designed. In the pass-band with corner frequency $\omega_p=0.4\pi$ the maximum ripple has to be smaller than $A_p=0.01$ dB to fulfill the overall requirements. In the stop-band from 0.7π to π the minimum attenuation has to be $A_s=100$ dB. As described in [9] the pass-band requirements are mapped to respective requirements for the sub-filters approximating the Taylor coefficients. The stop-band requirements have to be fulfilled by all sub-filters. Using the well-known Remez-algorithm, which is e.g. implemented in a respective MATLAB-function, the respective sub-filters can be designed very easily. It turned out that a Farrow-structure with 5 branches is required to fulfill the specification, where the highest order of a sub-filter is N=44. Note that the sub-filter for k=0 is not degenerated anymore to a pure delay, since it also has to fulfill the stop-band requirements. Thus the implementation costs are considerably increased due to the stop-band

specification. The hardware requirements are about the same as for the filter described in [3], which was designed for a similar specification, however by using a completely different design method.

During the optimization process for the decimation stages, a number of different filter structures had been considered for the realization of the fractional delay filter. It turned out that a superior solution with respect to implementation costs and delay can be obtained, by optimizing the fractional delay filter just for the pass-band requirements and fulfilling the stop-band specification by an additional cascaded low-pass filter with fixed coefficients.

A fractional delay filter in Farrow structure with 5 branches and sub-filters of orders N=[5 4 5 4] was sufficient to fulfill the pass-band requirements. Fig. 4 shows the group delay characteristic for values of Φ in the range of –0.3 to 0.5. The stop-band requirements can be fulfilled by a 34th-order linear phase FIR-filter, taking also the degradation due to the finite word-lengths of the coefficients into account. Using an approximately linear phase WDF-filter such as in stage 2 the hardware costs and the delay can be further reduced.

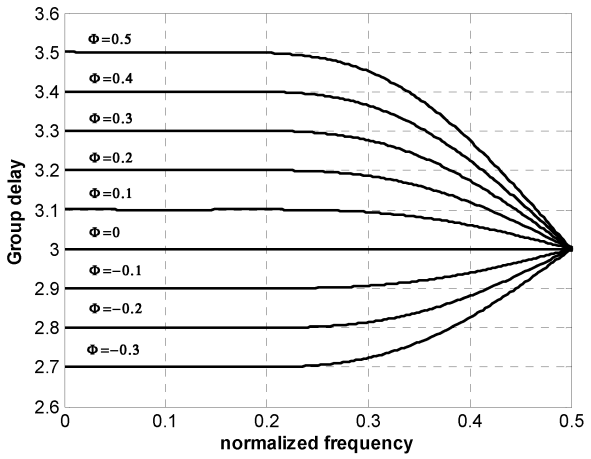

Fig. 4: Frequency characteristic of the fractional delay filter for values of Φ in the range of –0.3 to 0.5.

6. CONCLUSIONS

Next generation mobile systems will be based on multimode, multi-band, and multifunctional wireless systems which can be reconfigured by software-updates. Thus reconfigurable architectures for wireless networks and terminals are required, which can be obtained by shifting classical analogue signal processing into the digital domain.

In this contribution the design and optimisation of the digital filter stages for a flexible digital receiver had been presented. The decimation filters are very critical functional blocks with respect to hardware costs, power consumption, and delay in such a receiver. It has been shown that a very flexible and nevertheless optimised solution with respect to implementation costs, system delay and power consumption can be obtained by using a special kind of wave digital filters for the decimation stages. Furthermore the design and optimisation of a fractional delay filter needed for non-integer decimation ratios, is described. Several options for this filter had been considered in order to find the best solution for software defined radio receiver.

Due to the very limited number of multiplications the filter stages are well-suited for an ASIC- or FPGA-implementation. Compared to a classical solution based on linear phase FIR-filters the hardware costs could be reduced by more than 60% and the group delay is reduced by about 50%.

7. REFERENCES

[1] W. Tuttlebee, *Software Defined Radio, Enabling Technologies*, J. Wiley, New York, 2002.

[2] T. Hentschel and G. Fettweis, “Sample rate conversion for software radio,” *IEEE Communication Magazine,* vol. 38, no. 4, pp. 142-150*,* 2000.

[3] K. S. Yeung and S. C. Chan, “The Design and Multiplier-Less Realization of Software Radio Receivers With Reduced System Delay,” *IEEE Transactions on Circuits and Systems – I: Regular Papers,* vol. 51, no. 12, pp. 2444-2459*,* 2004.

[4] C. Dick and F.J. Harris, “Configurable Logic for Digital Communications: Some Signal Processing Perspectives,” *IEEE Communication Magazine*, vol. 37, no. 8, pp. 112-117, 1999.

[5] D. Brückmann, "Optimised Digital Signal Processing for Flexible Receivers", *Proc. ICASSP 2002,* Orlando, Fl., USA, 13.-17. Mai 2002.

[6] D. Brückmann, "Flexible Digital Receiver Architecture with Optimized Components", *Int. J. Electron. Commun*., vol. 55, no. 6, pp. 408-416, 2001.

[7] L. Gazsi, "Explicit formulas for lattice wave digital filters", *IEEE Trans. Circuits Systems,* vol. 32, no. 2, p. 68-88, 1985.

[8] J. Y. Kaakinen and T. Saramäki, “Design of Very Low-Sensitivity and Low-Noise Recursive Filters Using a Cascade of Low-Order Lattice wave Digital Filters”, *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing,* vol. 46, no. 7, pp. 906-914*,*1999.

[9] H. Johansson and P. Löwenberg, “On the Design of Adjustable Fractional Delay FIR Filters”, *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing,* vol. 50, no. 4, pp. 164-169, 2003.

[10] C. W. Farrow, A Continuously variable digital delay element, *IEEE Int. Symp. Circuits and Systems*, 1988, pp. 2641-2645.