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OPTIMIZED DIGITAL RECEIVER FOR FLEXIBLE WIRELESS TERMINALS

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ABSTRACT

The future development of mobile terminals will be driven by the enormous service potential of next generation systems and by the need to continuously widen the users choice with respect to access, service, and content by means of any terminal equipment.
In order to fit to these requirements novel architectural concepts for wireless systems are needed. In this contribution a flexible, digital receiver architecture with highly optimized components will be introduced. It will be shown how the A/D-converter and the filtering stages, which are the most critical components in such a receiver, can be optimized by using a properly designed $\Delta\Sigma$–modulator and novel digital filtering stages. These filtering stages perform decimation and channel selection together and consist of a special class of wave digital filters. Due to this concept a number of advantages are obtained and a very efficient realization in VLSI-technology becomes feasible.

1. INTRODUCTION

Recently a variety of architectures for software radio platforms have been presented in the literature [1, 2]. These architectures are designed to make mobile systems more flexible. Most of them are however not well-suited for future mobile terminals since they do not take restrictions with respect to low costs, low power consumption, and small size into account. Therefore in this presentation a flexible but also highly optimized receiver concept will be proposed, which accounts for all of these different requirements.
Flexibility with respect to the bandwidth requirements of different mobile standards can be obtained by performing channel selection in the digital domain, where it can be implemented by programmable digital filters. The A/D-converter in such a concept digitizes the wideband input signal, containing the desired channel together with the unwanted adjacent channel interferers. Very effective solutions are obtained when using $\Delta\Sigma$-modulators with oversampling for the digitization. In such a concept no additional filtering for channel selection is required since the adjacent channel interferers are suppressed by the decimation stages together with the high-pass shaped quantization noise. Furthermore the requirements to the anti-aliasing low-pass filter are reduced due to oversampling.

To account for low costs and low power the decimation filters must be optimized for an FPGA- or ASIC-implementation [1, 2]. Thus multiplications and MAC-operations should be avoided. Furthermore the decimation ratio of the filters should be adjustable so that the required flexibility with respect to the bandwidth and/or dynamic range is obtained. In order to allow the implementation of a fast AGC, which reduces the dynamic range requirements to the ADC, the group delay of the filters should be minimum. Finally no significant group delay distortion may be introduced in the passband.

Different types of filter structures for the decimation stages of $\Delta\Sigma$-modulators have been proposed in the literature [3, 4]. None of them however fulfills the above mentioned requirements completely. Therefore in this contribution novel decimation filters will be proposed, which better fit to the above requirements. It will be shown that a special class of lattice wave digital filters is very well suited for the lower decimation stages.

2. RECEIVER ARCHITECTURE

From a flexibility point of view, it is desirable to push the analog-to-digital boundary as close to the antenna as possible and implement all the signal processing digitally. Even though the development of ADCs and DSPs has made considerable advancements recently [1], more optimized solutions are required for a flexible mobile terminal. The main reason for this are the stringent cost and power consumption requirements of software defined radios in mobile terminals, which cannot be fulfilled by standard components. Thus a highly optimized solution is required, which however still has the flexibility needed for the application. Fig. 1 shows a block diagram of a software radio receiver architecture, which seems to be

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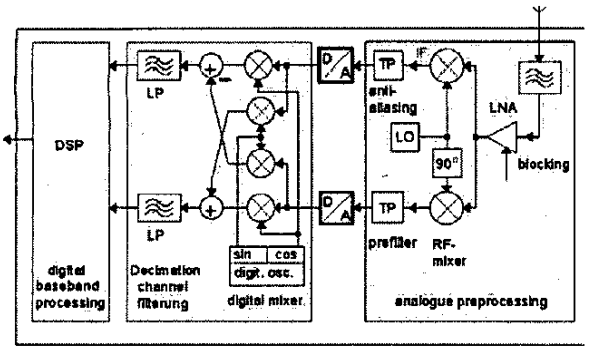

Fig. 1: Receiver architecture with broadband IF-sampling.

more appropriate for a mobile terminal. Obviously the structure is a mixed signal design with broadband analogue pre-processing and digital signal processing behind the A/D-converters. Whereas the analogue receiver front-end is relatively simple and mainly serves for low-noise amplification and frequency translation to an intermediate frequency (IF), the more complex signal processing is done digitally, e.g. channel filtering, demodulation, and detection.

Downconversion to the IF is performed by an I/Q-mixer, which rejects the nearby image component. By mixing down to a low IF, the problems of direct conversion receivers with DC-offset and 1/f-noise are avoided, whereas most of the advantages of direct conversion are retained. The input to the A/D-converters is a broadband signal containing the wanted signal together with adjacent channel interferers. Thus no external filtering by a bulky and costly saw-filter is required.

Critical parts are the A/D-converters, which must be broadband but nevertheless optimized with respect to costs and power consumption. In the next chapter it will be shown that $\Delta\Sigma$ modulators with oversampling are especially well suited for this application.

The digital part consists of two hardware blocks. The upper digital signal processing module, which operates at higher frequencies, is optimized with respect to chip area and power consumption, but nevertheless offers a certain degree of flexibility by using reconfigurable hardware. It can be implemented as an ASIC and/or FPGA. The main functions, which must be realized by this module, are downconversion of the A/D-converter output signal to baseband, higher frequency channel selection, and decimation. These functions require only a reduced flexibility even for multistandard capability, which can be obtained by the ASIC/FPGA implementation. The processor part is used for baseband signal processing and is highly flexible and easy to program.

3. OPTIMIZED $\Delta\Sigma$–MODULATOR

The resolution required for the ADCs of the digital receiver is determined by the dynamic range requirements of the receive path. Using an AGC in the RF-front end, the required dynamic range can be obtained from the smallest wanted and the largest unwanted signal which must be processed in common. The respective values can be found in the physical layer specifications of the various wireless and mobile standards as interferer and blocking requirements. By proper design of the analogue prefilters the most critical interferers are the 2nd adjacent channel signals. The blocker signals and the upper adjacent channels are attenuated already by the prefilters of 2nd- or 3rd-order thus relaxing the dynamic range requirements considerably. Furthermore, the minimum required signal-to-noise ratio for digital demodulation and detection must be added. Typical values for today's and future mobile systems like GSM, DECT and UMTS are dynamic requirements for the ADCs in the range of 65 to 75dB.

The performance of an A/D-converter with $\Delta\Sigma$–modulation is determined by its oversampling ratio *OSR*, the internal quantizer resolution B and the order N of the modulator. Furthermore the topology and the realized noise transfer function NTF(z) can have a strong influence on the performance. In a wireless receiver there are restrictions to the oversampling ratio however, due to power consumption requirements and due to the available clockfrequencies.

In order to minimize the hardware requirements for the quantizer, the DAC and the DSP-stages a one bit internal quantiser is used. Thus a $\Delta\Sigma$-modulator of higher order N is required. At first sight a band-pass modulator seems to be best suited to filter the wanted channel, which is a band-pass signal. Band-pass $\Delta\Sigma$–modulators, however, require twice the number of poles and zeros compared to its low-pass counterparts [3]. Thus, since the IF is low, a low-pass modulator with a notch of the noise-transfer function turns out to be the better choice.

With these restrictions a 3rd-order $\Delta\Sigma$ modulator with one bit quantizer, and the topology in fig. 2 has been identified as well suited for the application [5]. Due to the resonator with feedback coefficient g a notch of the noise transfer function is generated at a nonzero frequency, thus considerably improving the performance compared to classical designs [3, 5]. The complexity of the modulator is only slightly increased by the resonator.

Noise transfer functions with lowpass characteristic (e.g. butterworth or chebycheff) are already used widely in commercially available products. Considerable improvements compared to classical designs in the range of 5dB can be however obtained, by a newly developed coefficient optimization strategy described in [2]. The

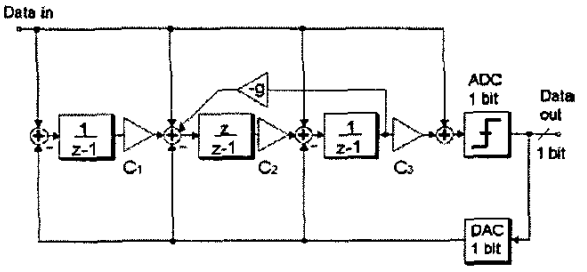

Fig. 2: ΔΣ-modulator of 3rd-order with notch of noise transfer function.

optimization procedure takes the bandpass characteristic of the input signal into account and places the notch at a frequency for optimal noise suppression in the band of interest. The optimal coefficient values for an oversampling ratio of 32 thus obtained are given as follows:

$$\{C_1, C_2, C_3, g\} = \{0.4, 0.375, 2, 0.012\}$$

These values result in a dynamic range of the modulator of about 73dB. The bandwidth of the A/D-converter can be adjusted in a wide range by adjusting the sampling frequency.

4. DIGITAL FILTERING STAGES

The required hardware for the decimation filters can be minimized by performing decimation in several stages with sample rate reduction after each stage, as shown in fig. 3. After ΔΣ–modulation of the IF-signal the complex mixer performs downconversion to baseband. Thus only real low-pass filters are required. The first stage performs decimation by a programmable factor M. The following 3 stages each reduce the sampling rate by a factor of 2. Each filter stage can be also bypassed, thus making the decimation ratio programmable in a large range.

The uppermost decimation stage is running at the highest clock frequency and therefore should be implemented by a very simple filter structure. Well-suited are cascaded integrator-comb (CIC) filters, which can be implemented by using only registers and adders.

For the lower decimation stages filters with a steeper transition band are required. Hardware efficient realizations can be obtained by using cascaded low-order bireciprocal lattice wave digital filters [6-8]. The respective transfer function is given by:

$$H(z) = 2^{-N} \prod_{i=i}^{N} [H_{i0}(z^2) + z^{-1} H_{i1}(z^2)] \quad (4.1)$$

where $H_{i0}(z)$ and $H_{i1}(z)$ are allpass filters.

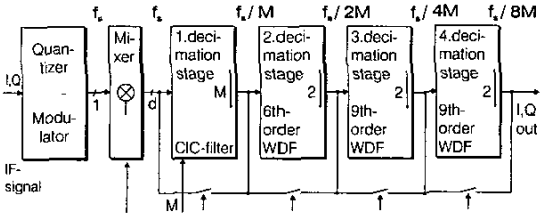

Fig. 3: Functional blocks in the receive path.

Using this filter type efficient decimators for sampling rate conversion by two can be obtained, since the number of coefficients to be implemented is reduced by 50% and the filter can run with the lower sampling frequency. Due to this cascade connection of low order WDFs a number of advantages are obtained, compared to existing solutions. Bireciprocal WDFs are minimum phase filters. They introduce however group delay distortion. By replacing one of the allpass sections by a pure delay a lattice WDF with approximately linear phase in the passband can be better approximated [7].

By cascading low-order sections a high stopband attenuation can be obtained with low coefficient sensitivity. Thus the optimized coefficients can be represented by very simple values so that no general multiplier is needed. Furthermore this structure is very modular, which is important for VLSI-implementation.

The architecture of the lattice wave digital filter for the 3rd and 4th decimation stages is shown in fig. 4. It consists of a cascade connection of three 3rd-order WDFs. For the 2nd decimation stage two 3rd-order cells are sufficient. All coefficients can be represented by a maximum of two shift-and-add operations, the respective optimized values are listed in table I.

Stage 2	Stage 3	Stage 4
$g_1 = 2^{-1} - 2^{-3}$	$g_1 = 2^{-1} - 2^{-4}$	$g_1 = 2^{-1} - 2^{-4}$
$g_2 = 2^{-1} - 2^{-3} - 2^{-5}$	$g_2 = 2^{-1} - 2^{-4}$	$g_2 = 2^{-1} - 2^{-4}$
----	$g_3 = 2^{-1} - 2^{-4}$	$g_3 = 2^{-1} - 2^{-4}$

Table I: Optimized filter coefficients for the dec. stages.

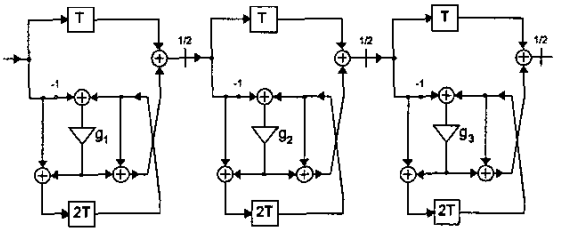

Fig. 4: 3 cascaded 3rd-order wave digital filters for use in the lower decimation stages.

Since the decimation by 2 is implemented with the last filter cell of each decimation stage, stage 2 can be realized by 4 registers and 11 shift-and-add operations. For the realization of the 3rd and 4th stage 7 registers, 12 adders and 3 shift-and-add operations are required.

5. PERFORMANCE RESULTS

Performance results of the receiver are shown by figs. 5 and 6. To analyze the behavior of the modulator in the presence of out of band signals in adjacent channels, two GMSK-modulated signals in the first and second adjacent channels had been used as inputs. Fig. 5 shows the modulator output spectrum thus obtained. The results confirm that neither the in-band-noise nor the out-of-band noise at the modulator output are considerably increased using broadband input signals, which are typical for the digital receiver concept considered.

The transfer functions of the lower decimation stages are shown by fig. 6. The 2nd filter stage consists of two cascaded bireciprocal lattice WDFs of order 3 each. The

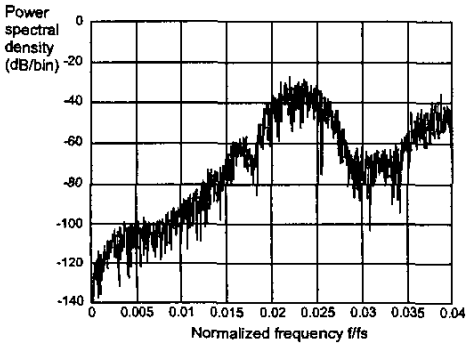

Fig. 5: Spectrum at modulator output with two GMSK-modulated adjacent channel signals.

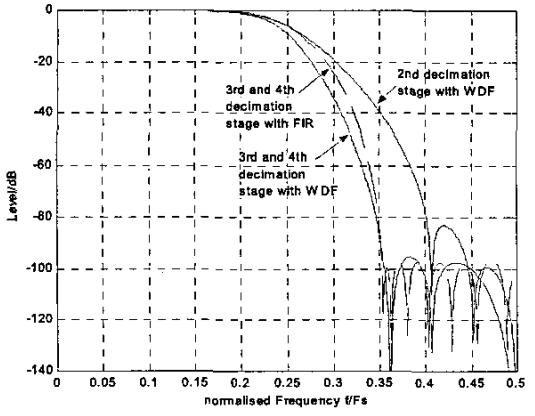

Fig. 6: Transfer functions of the lower decimation stages. 3rd and 4th filter stages are implemented using 3 cascaded 3rd-order WDFs. The attenuation requirements can be also fulfilled by an FIR-halfband-filter of order 27. The respective transfer characteristic is also shown in fig. 6 for comparison purposes. When cascaded the minimum stopband attenuation of the three lower decimation stages is 96dB.

6. CONCLUSIONS

The design and optimization of the components for a flexible digital receiver for use in wireless communications systems has been presented. The optimization process includes the modulator of the ΔΣ-A/D-converter, and the filter stages. The components have been optimized for a cost effective, combined FPGA/ASIC and processor implementation with the flexibility required by the application. The receiver concept is based on a low-IF architecture with channel filtering in the digital domain to allow flexibility and a complete integration of RF and baseband functionalities into a single integrated circuit in CMOS.

7. REFERENCES

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