OPTIMIZED DIGITAL SIGNAL PROCESSING FOR FLEXIBLE RECEIVERS

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ABSTRACT

To cope with the requirements of future mobile systems, the terminals must become more flexible with respect to multi-standard and multi-service capabilities. The flexibility and the degree of integration can be increased by replacing analogue by digital signal processing. To account also for the stringent cost and low power requirements the digital signal processing in such a concept must be optimized for a hardware efficient VLSI-implementation.

In this contribution the digital signal processing for a flexible and optimized receiver architecture will be considered. It consists of an optimized digital mixer and novel high-order, programmable decimation filters. For the lower decimation filter stages a structure of cascaded low-order wave digital lattice filters will be proposed. The use of this filter type results in a number of advantages compared to state of the art solutions.

1. INTRODUCTION

A variety of architectures for designing a software radio platform has been presented in recent literature [1, 2]. These concepts are developed to make mobile systems more flexible. Most of them are however not well-suited for future mobile terminals since low costs, low power consumption, and small size are additional restrictions for terminals which must be also met. Thus in this presentation the digital signal processing for a flexible but also highly optimized receiver concept will be considered, which accounts for all of these different requirements.

Multi-standard capability can be achieved by performing channel selection in the digital domain using programmable digital filters. In such a concept the wideband input signal containing the desired channel together with the unwanted adjacent channel interferers is digitized. Very effective solutions are obtained when using ΔΣ-modulators with oversampling for the A/D-conversion. In such a concept no additional filtering for channel selection is required since the adjacent channel interferers are suppressed by the decimation stages together with the high-pass shaped quantization noise. Furthermore the requirements to the anti-aliasing low-pass filter are reduced due to oversampling.

For optimum performance and minimum hardware costs some requirements to the digital mixer and the decimation stages should be also taken into account for the filter design.

For an cost effective and low power realization the filters should be optimized for an FPGA- or ASIC-implementation [2]. Thus multiplications and MAC-operations, available in a general purpose DSP, should be avoided. Furthermore the decimation ratio of the filters should be adjustable so that the required flexibility with respect to the bandwidth and/or dynamic range is obtained. In order to allow the implementation of a fast AGC, which reduces the dynamic range requirements to the A/D-converter, the group delay of the filters should be minimum. Finally no significant group delay distortion may be introduced in the passband.

Various filter structured had been proposed for the decimation stages of ΔΣ-modulators [3]. All these solutions however do not fulfill the above mentioned requirements completely. Therefore in this contribution novel decimation filters will be proposed, which better fit to the above requirements. It turns out that properly designed cascaded low order lattice wave digital filters are especially well suited for the lower decimation stages.

2. DIGITAL SIGNAL PROCESSING STAGES

Fig. 1 shows the architecture of the digital part of the receive path [4]. Quadrature down conversion of the broadband receive signal to a low IF is performed in the analogue domain. The I and Q components of the IF-signal are digitized then by ΔΣ-modulators. The complex digital mixer converts the signal down to baseband.

Sample rate reduction and channel-selection is then performed by the decimation filters, together with the suppression of the highpass-shaped quantization noise. It is well-known that the hardware required for the decimation filters can be minimized by performing decimation in several stages, with sample rate reduction

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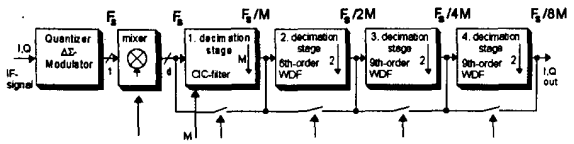

Fig. 1: Receive path with digital mixer and decimation filters.

decimation in several stages, with sample rate reduction after each stage, as shown in fig. 1. Whereas the first filter stage performs decimation by a programmable factor M, the lower 3 stages each reduce the sampling rate by a factor of 2.

The decimation ratio is programmable in a wide range since each decimation stage can be also bypassed, and the decimation factor M of the upper stage is adjustable. Since the decimation filters are designed such that the lowest stage fulfils the most stringent attenuation requirements, bypassing of one or two lower stages should be performed such that stage 4 is bypassed at first and then the preceding stages.

The uppermost decimation stage is running at the highest clock frequency and therefore should be implemented by rather simple filter structures for minimum costs and power consumption. Simple hardware structures can be obtained by using cascaded integrator-comb (CIC) filters which can be implemented by using only registers and adders. The stopband attenuation of the decimation filters are designed to fulfill the attenuation requirements of a 4th-order ΔΣ-modulator, which requires in the first stage a classical 5th-order CIC filter.

For the lower decimation stages filters with a steeper transition band are needed. Very hardware efficient realizations are obtained by using optimized bireciprcal wave digital filters, as described in the following.

3. IMPLEMENTATION OF THE DIGITAL MIXER

Due to the small wordlength b of the input signals I_i and Q_i (2x1bit), a very efficient realization of the digital quadrature mixer is obtained by using table look up techniques, as shown in fig. 2. The output signals I_o and Q_o of the mixer are obtained from I_i and Q_i, the mixing frequency F_{IF}, and the sampling frequency F_s, according to following relationships:

$$I_0 = I_i \bullet \cos(2\pi \frac{F_{IF}}{F_S} n) - Q_i \bullet \sin(2\pi \frac{F_{IF}}{F_S} n), \quad (3.1)$$

$$Q_0 = I_i \bullet \sin(2\pi \frac{F_{IF}}{F_S} n) + Q_i \bullet \cos(2\pi \frac{F_{IF}}{F_S} n), \quad (3.2)$$

with n = 0,1,2,3,4,... .

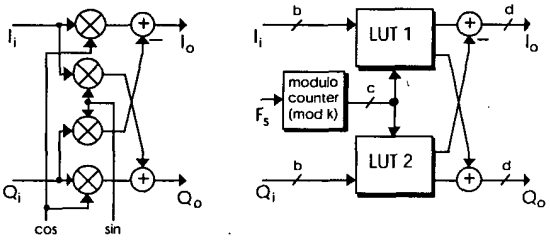

Fig. 2: Realization of the digital quadrature mixer using table look up techniques.

The wordlength c of the counter output in fig. 2 is given by $c=\log_2(k)$, with $k=F_s/F_{IF}$ the modulus of the counter. Thus with d as the wordlength of the mixer output signals, the wordlength of each LUT output must be d-1. Taking the symmetries of sine and cosine into account, the required size N of each look-up table is given by:

$$N = \tfrac{1}{2} \cdot 2^{(b+c)} \cdot (d-1) \ \text{[Bits]}. \quad (3.3)$$

The output wordlength d determines the distortion introduced by the mixer and should be chosen such that the signal to noise ratio of the modulator output is not considerably increased in the frequency band of interest by the mixing operation. Typical values for the digital receiver are b=1, k=128, c=7 and d=8, resulting in two look-up tables of 128x7bits each.

4. DECIMATION FILTERS WITH WDFs

The lower decimation stages can be very efficiently implemented by cascaded low-order bireciprocal lattice wave digital filters. Bireciprocal lattice wave digital filters are a special case of lattice WDFs and have a symmetrical filter characteristic with respect to ¼ of the sampling frequency [5]. The transfer function of N cascaded bireciprocal lattice wave digital filters is given by following relationship:

$$H(z) = 2^{-N} \prod_{i=i}^{N} [H_{i0}(z^2) + z^{-1} H_{i1}(z^2)], \quad (4.1)$$

where $H_{i0}(z)$ and $H_{i1}(z)$ are all-pass transfer functions.

Using this cascade connection of low order WDF sections results in a number of advantages compared to existing solutions [6-8].

At first the realization costs are low since the number of coefficients to be implemented is reduced by 50% and the filter can run with the lower sampling frequency.

Bireciprocal WDFs are minimum phase filters. They introduce however group delay distortion. By replacing

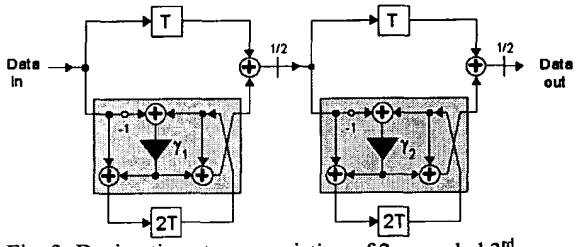

Fig. 3: Decimation stage consisting of 2 cascaded 3rd-order bireciprocal wave digital filters.

one of the all-pass sections by a pure delay a lattice WDF with approximately linear phase in the passband can be obtained. This holds since in the passband of the filter the responses of the all-pass subfilters must be approximately equal. Since one of the branches is a pure delay, the phase response of the overall filter has approximately a linear phase in the passband. This will be taken into account by cascading 3rd-order cells of bireciprocal lattice wave digital filters, as shown in fig. 3, resulting in a superior group delay performance compared to a direct realization of a lattice WDF.

By cascading low-order sections a high stopband attenuation can be obtained with low coefficient sensitivity. Thus the optimized coefficients can be represented by very simple values and a wordlength of only a few bits is required. Due to the very simple coefficient representation, no general multiplier is needed, thus minimizing the implementation costs again. Furthermore the shorter wordlength also holds for the signal representation, resulting in reduced implementation costs for the adders and registers. Since the cascaded low-order sections are very modular, they are well suited for VLSI-implementation.

The architecture of the lattice wave digital filter for the 2nd decimation stage is shown in Fig. 3. It consists of a cascade of two 3rd-order bireciprocal WDF filter blocks, resulting in a total filter order of 6. The decimation by two can be also performed at the filter input as shown in fig. 4. This filter structure can thus be clocked with the reduced sampling rate.

The 3rd and 4th decimation stages must fulfill higher attenuation requirements which can be met by a cascade of three 3rd-order cells resulting in a total filter order of 9. All coefficients can be represented by a maximum of two shift-and-add operations, the respective optimized values are listed in table I.

Stage 2	Stage 3	Stage 4
$\gamma_1 = 2^{-1} - 2^{-3}$	$\gamma_1 = 2^{-1} - 2^{-4}$	$\gamma_1 = 2^{-1} - 2^{-4}$
$\gamma_2 = 2^{-1} - 2^{-3} - 2^{-5}$	$\gamma_2 = 2^{-1} - 2^{-4}$	$\gamma_2 = 2^{-1} - 2^{-4}$
----	$\gamma_3 = 2^{-1} - 2^{-3}$	$\gamma_3 = 2^{-1} - 2^{-3}$

Table I: Optimized filter coefficients for the decimation stages.

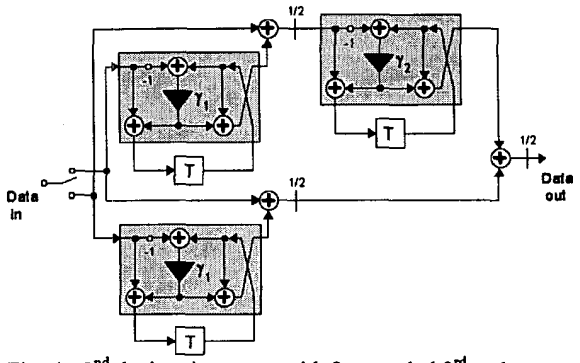

Fig. 4: 2nd decimation stage with 2 cascaded 3rd-order WDFs and sample rate reduction by 2 at the input.

Since the decimation by 2 is implemented at the filter input decimation stage 2 can be realized by 3 registers, 11 adders and 4 shift and operations. A wordlength of only 6 bits is required for the coefficient representation.

For the realization of the 3rd and 4th stage 6 registers, 15 adders, and 5 shift and add operations are needed for each stage. For the respective coefficients a wordlength of only 5 bits is required.

The attenuation requirements of the 4th decimation stage is also fulfilled by a classical 9th-order bireciprocal WDF, which requires however 4 registers, 13 adders and 12 shift and add operations. Especially the necessary wordlength of 12 bits for the coefficient representation results in increased hardware costs.

Furthermore the attenuation requirements can be also fulfilled by an FIR-halfband filter of order 27, with 15 coefficients unequal to zero. For the coefficient representation a wordlegth of about 20 bits is necessary. Thus this filter type results in more hardware costs and additional group delay. The results show that, compared to classical solutions, a considerable hardware reduction has been obtained using the cascaded low order sections.

5. SIMULATION RESULTS

Fig. 5 shows the frequency responses of the lower decimation stages. The 2nd filter stage consists of two cascaded 3rd-order bireciprocal lattice WDFs of order 3 each. The 3rd and 4th filter stages are implemented by 3 cascaded 3rd-order WDFs. The transfer characteristic of a 27th-order FIR-halfband filter is also shown in fig. 5. It fulfills the requirements of the 3rd and 4th filter stages too, but needs considerably more hardware for implementation.

Fig. 6 shows the overall frequency response of the three lower decimation stages. A minimum attenuation of 96dB is obtained. Together with the first decimation stage, the minimum attenuation is even higher.

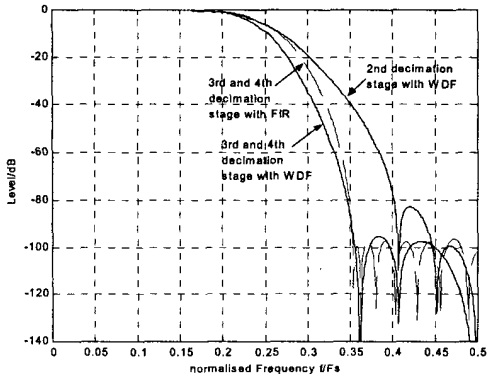

Fig. 5: Frequency responses of the lower decimation stages

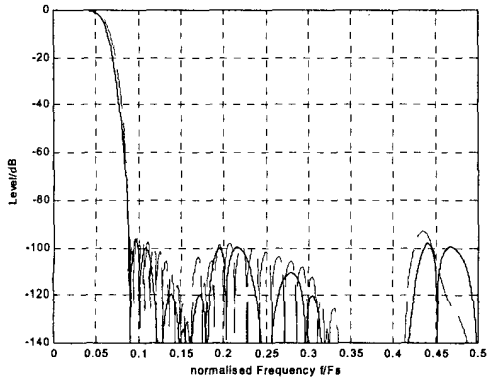

Fig. 6: Overall frequency response of the three lower decimation stages,
solid line: cascaded low order WDFs,
dashed line: FIR-halfband filters.

Due to the excellent passband performance of bireciprocal WDFs, the ripple is smaller than 0.02 dB which is sufficient for the application. The passband droop could be further reduced by a simple first order attenuation equalizer, if the filters are to be used in other applications.

The resolution required for the ADCs of the digital receiver is determined by the dynamic range requirements of the receive path. If the RF-front end is designed properly, the required dynamic range can be obtained from the smallest wanted and the largest unwanted signal which must be processed in common. The respective values can be found in the physical layer specification of the various wireless and mobile standards as interferer and blocking requirements.

6. CONCLUSIONS

In this contribution optimized digital signal processing stages required in a flexible receiver architecture were presented. The proposed digital part of the receiver contains an optimized digital mixer and novel high-order, programmable decimation filters. It has been shown that very effective realizations for the lower decimation stages can be obtained, by using cascaded low-order wave digital filters. This filter type can be implemented with minimum hardware compared to other solutions such as classical wave digital filters or FIR-filters.

Further advantages of the proposed filter structures are superior sensitivity properties with respect to coefficient quantization effects, better noise performance and less group delay distortion compared to classical structures.

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