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Flexible Digital Receiver Architecture with Optimized Components

Dieter Brückmann

Dedicated to Professor Alfred Fettweis on the occasion of his 75th birthday

Abstract **Future wireless communication systems require increased flexibility, lower power consumption, smaller size and decreasing costs for the terminals and therewith for the components. By replacing analogue by digital signal processing the degree of integration and the flexibility of a terminal with respect to multi-mode capability can be improved. In a highly integrated implementation the most critical components are the A/D-converter and the digital filter stages due to high speed and low power requirements. In this contribution a novel concept for a flexible, digital receiver with highly optimized components will be presented. The concept is based on down-conversion of the broadband receive signal to a low intermediate frequency. The main modules of the receiver are a properly designed $\Delta\Sigma$-modulator for A/D-conversion, and novel digital filtering stages. It will be demonstrated, that the use of cascaded low-order wave digital lattice filters results in a number of advantages and makes a very efficient realization in VLSI-technology feasible.**

Keywords **Digital receiver, Software radio, $\Delta\Sigma$-modulator, Wave digital filters**

1. Introduction

In the field of mobile communications a number of new services and applications will come up in the next years, which will be covered by a variety of existing or new standards. These standards can have very different requirements with respect to bandwidth, dynamic range and so forth. Thus flexible but low cost terminals with low power consumption and small size will be needed in the future.

In order to account for these requirements novel architectures and circuit techniques must be developed to increase the degree of integration and the programmability of RF-transceivers. Higher integration will reduce costs and power consumption and can be obtained by novel transceiver concepts avoiding external components such as saw filters. By moving channel selection into the digital domain, where it can be implemented by programmable digital filters, multi-standard capability can be achieved. The A/D-converter in such a concept must digitize the wideband input signal containing the desired channel together with the unwanted adjacent channel interferers.

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$\Delta\Sigma$-modulators with oversampling are especially well suited for this application because the adjacent channel interferers are filtered out by the decimation stages together with the high-pass shaped quantization noise. Thus, no additional filtering for channel selection is required. A further advantage results from the reduced requirements to the anti-aliasing filter due to over-sampling.

In this paper the optimized components for such a receiver architecture will be described, which can be used in a flexible, low-cost mobile terminal with low power consumption. The $\Delta\Sigma$-modulator topology of the A/D-converter has been combined with digital filter stages which are optimized with respect to the requirements in reconfigurable digital receivers.

Sampling is performed at a relatively low intermediate frequency. Unwanted mirror signals are avoided by quadrature signal processing so that sampling of the I- and Q-components is required using two ADCs in parallel. The input signal to the A/D-converters contains adjacent channel signal components in addition to the desired signal. Since the desired signal can be a band-pass signal situated at a low intermediate frequency, the classical low-pass $\Delta\Sigma$-modulator with all zeros of the noise transfer function at zero frequency is not the optimal choice. Thus a $\Delta\Sigma$-modulator was developed using a novel design method for the design of optimal $\Delta\Sigma$-modulators with notches of the noise transfer function. It shows considerably better performance than conventional designs [1].

To obtain optimum performance for the receiver together with minimum hardware effort, the decimation stages must fulfil some requirements, which should be taken into account during the filter design process. To account for the very stringent cost and low power requirements in a mobile terminal, the decimation filters have to be be optimized for a FPGA- or ASIC-implementation [2–4]. Thus multiplications and MAC-operations, available in a general purpose DSP, should be avoided. To obtain the required flexibility with respect to the bandwidth and/or dynamic range, the decimation ratio of the filters should be adjustable. To allow the implementation of a fast AGC in the receiver, the group delay of the filters should be minimum. Furthermore no significant group delay distortion may be introduced in the pass-band.

The various filter structures proposed in the literature for the decimation stages of $\Delta\Sigma$-modulators (see e.g. [5, 6]) do not fulfill the above mentioned requirements completely. Therefore in this paper novel decimation filters will be proposed, which better fit the above requirements. It will be shown that properly designed cascade

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connections of low order lattice wave digital filters are especially well-suited.

Lattice wave digital filters consist of a parallel connection of all-pass sections [7, 8]. They have several advantageous properties, such as low coefficient sensitivity in the pass-band, low roundoff noise and the absence of parasitic oscillations. Furthermore they are minimum phase recursive filters.

A disadvantage however can be the high sensitivity in the stop-band with respect to the coefficient truncation. For a high stop-band attenuation many bits are required for the coefficient representation. This problem can be avoided by using cascade connections of low order wave digital sub-filters [9, 10], as will be shown in this contribution. Furthermore it will be shown that group delay distortion in the pass-band, typical for recursive filters, can be drastically reduced by implementing one of the all-pass sections by a pure delay.

2. Receiver architecture with IF-sampling

The straight forward way to implement a software defined radio is to put fast A/D- and D/A-converters as close as possible to the antenna and implement all the signal processing digitally. Even though the development of standard components, such as ADCs and DSPs, which are essential for such a concept, has made considerable advancements in the last years [11, 12], more optimized solutions are required for a flexible mobile terminal. The main reason for this are the stringent cost and power consumption requirements of software defined radios in mobile terminals, which cannot be fulfilled by off-the-shelf standard components. Thus a highly optimized solution is required, which however still has the flexibility necessary for the application.

Fig. 1 shows a block diagram of the digital receiver architecture, which seems to be more appropriate for a mobile terminal. The RF signal at the antenna is filtered by a simple blocking filter and is then amplified by the low-noise amplifier (LNA). Down-conversion to the intermediate frequency is done using an I/Q-mixer which has to reject the nearby image components. By mixing down to a low IF, the problems of direct down conversion receivers (zero-IF or homodyne receivers) with DC-offset and $1/f$ noise are avoided [13, 14]. The input to the A/D-converters is a broadband signal containing the wanted signal and the unwanted interference of the adjacent channels, as shown in Fig. 2. Thus no external channel filtering, using a costly and bulky saw filter, is required. The IF should be as low as possible to reduce the bandwidth requirements to the A/D-converters.

In a conventional band-pass IF-structure the input signal is down-converted to the IF as a real signal after preprocessing by fairly simple analogue bandpass filters. These pre-filters must be operated at a very high frequency however and cannot be integrated. Furthermore in such a classical heterodyne receiver the IF must be rather high to obtain the required mirror signal suppression with low-order pre-filters. Typical values for the IF are in the range of 5%–10% of the carrier frequency. Thus the intermediate frequencies of receivers for mobile standards like DECT or GSM are in the range of 100 MHz. Since digitization at such high frequencies is very costly, signal processing, such as channel selection, is normally done in the analogue domain.

Using the "low-IF-concept" several advantages are obtained compared to the classical solution. Especially the intermediate frequency can be chosen considerably smaller as shown in Fig. 2. The IF is in the range of the channel bandwidth, thus a suitable value for DECT is 864 kHz. Therefore the pre-filters can be easily integrated as switched capacitor or active RC-filters. Mirror signal suppression is obtained by quadrature signal processing. Furthermore digitization can be performed very efficiently at this low IF, so that more complex signal processing can be done in the digital domain. A possible drawback of this "low-IF-architecture" is the higher sensitivity with respect to mirror signal suppression. It has been shown however, that image reject mixers with sufficient performance can be implemented in CMOS technology [14]. After pre-filtering by simple analogue anti-aliasing filters of 2^{nd}- or 3^{rd}-order the A/D-conversion is performed. By using a $\Delta\Sigma$-modulator the sampling frequency is much higher

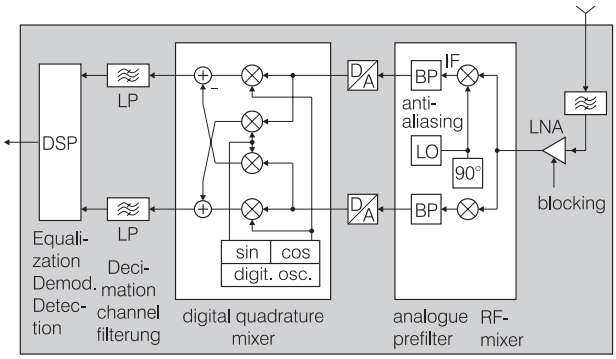

Fig. 1. Receiver architecture with broadband I/F-sampling

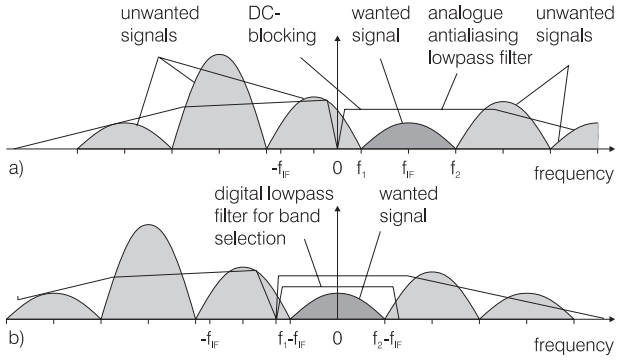

Fig. 2. Scheme for down-conversion and channel selection filtering at the IF, (b) and after down-conversion to baseband.

than the frequency band of interest, which is situated in the frequency interval $[f_1, f_2]$ (see Fig. 2) with

$$f_1 = f_{IF} - \frac{\Delta f}{2},\ f_2 = f_{IF} + \frac{\Delta f}{2},$$

where f_{IF} is the intermediate frequency and Δf the signal bandwidth.

At first sight a band-pass modulator seems to be best suited to filter the wanted channel, which is a band-pass signal. Band-pass $\Delta\Sigma$-modulators however, require twice the number of poles and zeros compared to its low-pass counterparts [5]. Thus, since the IF is low, a low-pass modulator turns out to be the better choice.

After digitization by the modulator, the signal spectrum is down-converted to baseband using a digital complex or quadrature mixer, as shown in Fig. 1. By this operation no image components are mirrored into the signal band. The channels in the frequency band of interest are shown in Fig. 2b after down-conversion. Finally, decimation and channel filtering can be performed by digital low-pass filters.

3. Design of $\Delta\Sigma$-modulators

Classical $\Delta\Sigma$-modulators with N cascaded integrators [5], only have zeros of the noise transfer function for z = 1. For this modulator type the noise transfer function is given as follows:

$$NTF(z) = \left(1 - z^{-1}\right)^N, \tag{1}$$

with N the order of the modulator. The respective realization is shown in Fig. 3, the coefficients C_i can be chosen such that relationship (1) holds. The theoretically obtainable dynamic range DR of an N^{th}-order $\Delta\Sigma$-modulator with low-pass characteristic and a usable band from $-f_2$ to $+f_2$ is given by following relationship [5]

$$DR = \frac{3}{2}\left(2^B - 1\right)^N \frac{2N+1}{\pi^{2N}} OSR^{2N+1}, \tag{2}$$

with $OSR = f_s/2f_2$ the over-sampling ratio and f_s the sampling frequency of the A/D-converter. B corresponds to the resolution of the internal quantizer.

To make the analogue part of the A/D-converter simple, we restrict the resolution B of the quantizer in the following to 1 bit. Using eq. (2) the achievable dynamic range and the equivalent resolution in bits for $\Delta\Sigma$-modulators are listed in Table 1 for several over-sampling ratios.

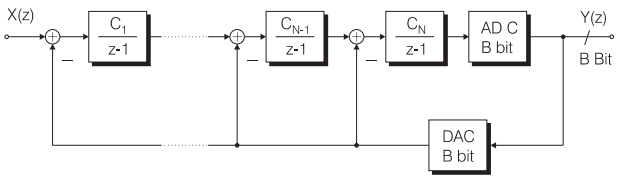

Fig. 3. N^{th}-order $\Delta\Sigma$-modulator with integrating noise transfer function.

Table 1. Dynamic range and equivalent resolution of ideal $\Delta\Sigma$-modulator with integrating noise transfer function and binary quantizers. N is the order of the modulator.

OSR	$N=1$	$N=2$	$N=3$	$N=4$
4	15 dB/ 2 Bits	19 dB/ 3 Bits	23 dB/ 3 Bits	26 dB/ 4 Bits
8	24 dB/ 4 Bits	34 dB/ 5 Bits	44 dB/ 7 Bits	62 dB/ 10 Bits
16	33 dB/ 5 Bits	49 dB/ 8 Bits	65 dB/ 10 Bits	95 dB/ 15 Bits
32	42 dB/ 7 Bits	64 dB/ 10 Bits	86 dB/ 14 Bits	128 dB/ 21 Bits
64	51 dB/ 8 Bits	79 dB/ 13 Bits	107 dB/ 17 Bits	161 dB/ 26 Bits

This table will be used in the following as the starting point for performance estimation of the different modulator architectures for use in the digital receiver. Note that the values in Table 1 are upper bounds for the dynamic range. It is well known that $\Delta\Sigma$-modulators of orders N greater than two are not stable when using binary quantizers and a noise transfer function according to eq. (1) [5]. It has been shown however that higher order modulators can be made stable by using modified noise transfer functions with a limited gain at higher frequencies [5, 15]. A possible solution is a noise transfer function $NTF(z)$ with butterworth high-pass characteristic, the maximum value of which is limited to $NTF_{max} = 1.5$ [5]. In order to make the modulator realizable, the leading coefficient of the numerator and denominator polynomials of $NTF(z)$ must be set to 1. The noise transfer function can now be expressed by the following equation:

$$NTF(z) = 1/\left[1 + \sum_{i=1}^{N} A_i \left(\frac{1}{z-1}\right)^{N-i+1}\right], \tag{3a}$$

$$A_i = K \prod_{j=i}^{N} C_j. \tag{3b}$$

It is noteworthy that this noise transfer function can be directly implemented using the structure in Fig. 3 with the integrator coefficients C_i and the quantizer gain K. In the frequency band of interest, where $f \ll f_s$ or equivalently $|z-1| \ll 1$ for $z = \exp(j2\pi f/f_s)$ holds, the noise transfer function can be approximated by:

$$|\ NTF(z)\ | \approx \frac{(z-1)^N}{A_1} \tag{4}$$

Thus, compared to (1) the noise is increased by $1/{A_1}^2$ reducing the dynamic range by ${A_1}^2$ as well. With eq. (3a)

Table 2. Characteristic parameters of $\Delta\Sigma$-modulators with butterworth high-pass characteristic for the noise transfer function.

N	1	2	3	4
f_c/f_s	0.1476	0.0917	0.0645	0.0495
A_1	0.667	0.5585	0.110	0.0154
O_L	0.95	0.86	0.6	0.45
$Loss L_B{}^*$	4 dB	6 dB	24 dB	43 dB

and with $NTF_{max} = 1.5$ the cutoff frequency f_c of the butterworth high-pass filter is fixed for a given filter order N. f_c normalized to the sampling frequency f_s is tabulated in Table 2, together with the respective values for A_1. Furthermore, in order to avoid overload, the input signal level must be limited to a value O_L. Simulations with discrete time models of the modulators show that low frequency and/or DC input signals are the most critical with respect to overload. Thus the O_L values listed in Table 2 had been obtained by simulations taking into account an additional safety margin of 10% for such input signals. The dynamic range is therefore reduced by the value L_B compared to eq. (2), with L_B and L_B* given by:

$$L_B = 1/(A_1 O_L)^2 \tag{5}$$

$$L_B^* = -20 \log (A_1 O_L) \tag{6}$$

Values for L_B^* are also listed in Table 2. Even though stability is given also for higher order modulators, the severe loss in dynamic range, compared to the values listed in Table 1, makes this type of noise transfer function not the optimal solution for A/D converters in digital receivers.
A more efficient method for the design of higher order $\Delta\Sigma$-modulators with binary quantizers was proposed in [15], where values of 1/5 and 1/25 for a 3^{rd}-order and 4^{th}-order topology were proposed for A_1 to assure stability. Thus, for this modulator type the dynamic range is reduced by a smaller loss $L = 1/\left(A_1^2.O_L^2\right)$. The O_L values had been obtained by the same method as described above. The respective values for L^* are given in Table 3 for modulator orders N of 1 to 4.

Table 3. Characteristic parameters of optimized, realizable $\Delta\Sigma$-modulators with 1 bit quantizers.

N	1	2	3	4
A_1	1	1	0.2	0.04
O_L	0.95	0.86	0.55	0.45
$Loss L^*$	0.4 dB	1.3 dB	19 dB	35 dB

4. Design of $\Delta\Sigma$-modulators with resonators

An alternative approach to higher order $\Delta\Sigma$-modulators is to distribute the zeros of the noise transfer function across the signal band rather than just at DC. If done properly this may more efficiently shape the quantization noise out of the band of interest. This approach seems to be particularly useful for the A/D converter in the digital receiver, because the over-sampling ratio must be rather low due to power savings requirements. Fig. 4 shows a flexible $\Delta\Sigma$-modulator architecture for the realization of an N^{th}-order $\Delta\Sigma$-modulator, consisting of a cascade of N-M integrators and M resonators with feedback paths. This topology can be used for the realization of noise transfer functions with N-$2M$ zeros at DC and M pairs of zeros at finite positive frequencies [1, 5]. The resonant frequencies f_i of the noise transfer function are determined by the coefficients g_i in the feedback paths of the resonators. They can be computed by following relationship, when the scaling coefficients C_i are already fixed:

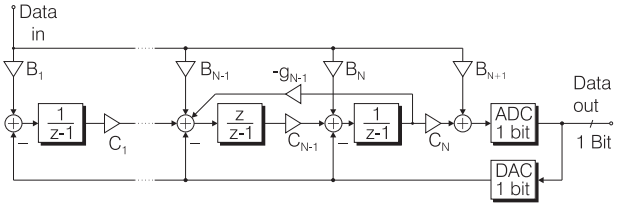

Fig. 4. $\Delta\Sigma$-modulator topology of N^{th}-order with M pairs of noise transfer function zeros at $z \neq 1$ and N-$2M$ noise transfer function zeros at $z = 1$.

$$g_i = (2\pi f_i / f_s)^2 / C_i \,, \tag{7}$$

with f_s the sampling frequency. It is apparent that some of the loss due to the modified noise transfer function can be recovered by spreading the zeros of $NTF(z)$ across the band of interest so that the in-band noise is minimized. The feed-forward paths with coefficients B_i are implemented in order to make the design of the signal transfer function $STF(z)$ independent of $NTF(z)$. For the digital receiver $STF(z)$ should be designed with a low-pass characteristic so that out-of-band signals are suppressed already by the modulator. In the frequency band containing the wanted signal $|STF(z)|$ should be equal to 1. The noise transfer function of the structure in Fig. 4 can be described by:

$$NTF(z) = (z-1)^{N-2M} \prod_{i=1}^{M} \left[(z-1)^2 + z g_i C_i\right] / D(z), \tag{8}$$

where $D(z)$ is the denominator polynomial [5]. With $z = \exp(j\Omega)$ and with $|f| \ll f_s$ in the frequency band of interest, following relationships hold:

$$|z| = 1, \; |z-1| \approx |\Omega| \ll 1. \tag{9}$$

Thus, the noise transfer function can be approximated in the frequency band of interest by:

$$| NTF\left(e^{j\Omega}\right) |^2 = \Omega^{2N-4M} \prod_{i=1}^{M} | \Omega^2 + g_i C_i |^2 / A_1^2, \quad (10)$$

for $| \Omega | \ll 1$.

The noise can be minimized by minimizing this function in the pass-band of the modulator and using eq. (7). Respective optimized resonant frequencies f_i can be determined, resulting in coefficient values g_i. The improvement due to the resonators can be determined by using these values g_i in eq. (10) and by comparison with eq. (4). Compared to the noise transfer function with all zeros at $z = 1$ a noise reduction and thus an improvement of the dynamic range by a value of G can be obtained by an N^{th}-order modulator with one resonator, where G is given by:

$$G = (2N-1)^2/4. \quad (11)$$

G is listed in Table 4 for modulator orders of 2 to 4. Respective values for modulators with more than one resonator can be determined by a similar method. Thus a simple method is now available for quick performance estimation of $\Delta\Sigma$-modulators with different topologies and noise transfer functions.

Table 4. SNR gain due to one pair of noise transfer function zero at $z \neq 1$.

N	2	3	4
$G* = 10\log(G)$	3.5 dB	8 dB	11 dB

5. Optimized $\Delta\Sigma$-modulator for the digital receiver

The results of the preceding chapters are used in the following to identify an optimal $\Delta\Sigma$-modulator for the receiver architecture in Fig. 1. The resolution required for the ADCs of the digital receiver is determined by the dynamic range requirements of the receive path. If the RF-front end is designed properly, the required dynamic range can be obtained from the smallest wanted and the largest unwanted signal which must be processed in common. The respective values can be found in the physical layer specification of the various wireless and mobile standards as interferer and blocking requirements. Furthermore, the minimum required signal-to-noise ratio for digital demodulation and detection must be added. Typical values for mobile systems like GSM and DECT are dynamic requirements for the ADCs in the range of 65 to 75 dB.

The performance of a $\Delta\Sigma$-modulator is determined by its over-sampling ratio OSR, the internal quantizer resolution B and the order N of the modulator. Furthermore the topology and the realized noise transfer function $NTF(z)$ can have a strong influence on the performance. In a wireless receiver there are severe restrictions to the over-sampling ratio however, due to power consumption requirements and due to the available clock-frequencies. Over-sampling ratios of up to 128 are achievable values for today's wireless (TDMA) systems with a channel bandwidth in the MHz range and the available clock frequencies in mobile terminals.

The hardware requirements with respect to the quantizer, the DAC and the digital signal processing stages are minimized by using a one bit internal quantizer. Therefore, a $\Delta\Sigma$-modulator of higher order N is required. With these restrictions and using the design concept described previously, a 3^{rd}-order $\Delta\Sigma$-modulator with one bit quantizer, and the topology in Fig. 5 has been identified as well suited for the application. Due to the resonator with feedback coefficient g a notch of the noise transfer function is generated at a nonzero frequency, thus considerably improving the performance compared to classical designs [15].

Figure 6 shows the achievable dynamic range of a 3^{rd}-order modulator as a function of the over-sampling ratio. The values, which are obtained by using the values in Tables 1 to 4, are given for 4 different noise trans-

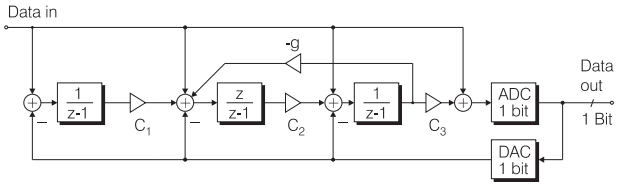

Fig. 5. 3^{rd}-order $\Delta\Sigma$-modulator with noise transfer function notch.

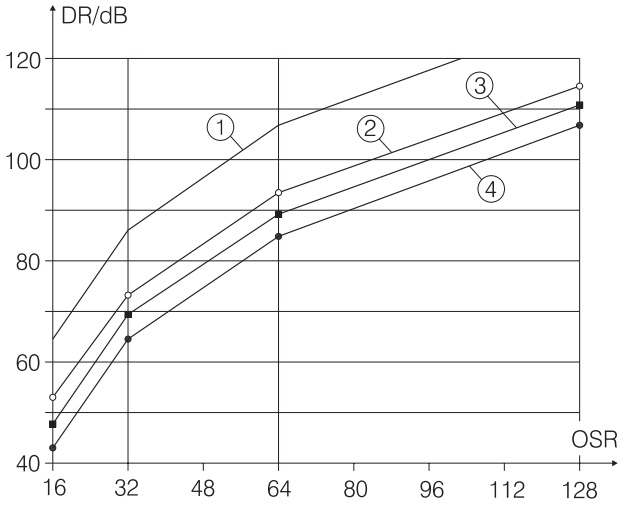

Fig. 6. Dynamic range of 3^{rd}-order $\Delta\Sigma$-modulators as a function of the over-sampling ratio OSR, (1) theoretical optimum, (2) optimized with notch, (3) butterworth characteristic with notch, (4) optimized without notch.

fer functions. Whereas curve 4 shows the performance of the modulator without resonator, curve 3 shows the improvement of about 4 dB obtained by the notch and a noise transfer function with butterworth characteristic. Noise transfer functions with butterworth characteristic are already used widely in commercially available products [12]. Further improvements in the range of additional 4 dB can however be obtained by the newly developed coefficient optimization strategy which is described in more detail in [1]. The respective values for the dynamic range are given by curve 2. Curve 1 in Fig. 6 shows the optimum theoretically obtainable by a 3^{rd}-order modulator. An implementation of the respective noise transfer function however results in unstable modulators, so that curve 2 corresponds to the optimum which is actually realizable. The respective optimized coefficient values for several over-sampling ratios are given by Table 5, together with the overload level O_L, the maximum SNR and the achievable dynamic range DR.

Table 5. Optimum coefficient values for 3^{rd}-order $\Delta\Sigma$-modulators with notch, respective signal to noise ratio SNR, and dynamic range DR.

OSR	C_1, C_2, C_3, g	SNR	DR	O_L
16	0.4, 0.4, 2, 0.0125	45 dB	52 dB	0.55
32	0.4, 0.375, 2, 0.0012	66 dB	73 dB	0.55
64	0.3, 0.5, 2, 0.00075	87 dB	93 dB	0.6
128	0.3, 0.5, 2, 0.00018	108 dB	114 dB	0.58

The sampling frequency of the modulator and therewith the over-sampling ratio can be made adjustable to account for flexibility. The dynamic range increases or decreases with increasing or decreasing over-sampling ratio respectively. The optimal resonant frequency however changes with the over-sampling ratio too. It can be adjusted by modifying the coefficient g.

The modulator can e.g. be implemented in switched capacitor technique. Thus the coefficient ratios correspond to capacitance ratios. By proper scaling of the capacitance values the maximum output voltages at the integrator outputs can be optimized. The notch frequency and the sampling frequency can be made adjustable by implementing several switchable capacitances for the coefficients.

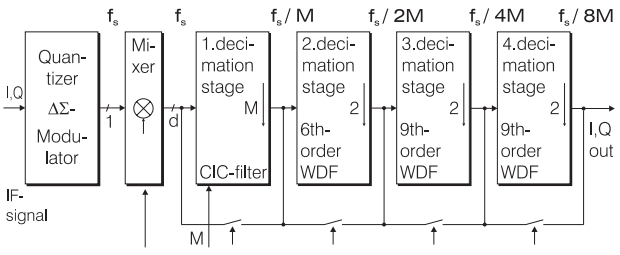

Fig. 7. Receive path with decimation filters.

6. Implementation of the digital filters

The required hardware for the decimation filters can be minimized by performing decimation in several stages with sample rate reduction after each stage. Such an architecture is shown in Fig. 7. After $\Delta\Sigma$-modulation of the IF-signal the complex mixer performs down-conversion to baseband. Thus only real low-pass filters are required for the decimation. The first stage performs decimation by a programmable factor M. The following 3 stages each reduce the sampling rate by a factor of 2. Each decimation stage can be also bypassed, so that the decimation ratio is programmable in a large range.

The uppermost decimation stage is running at the highest clock frequency and therefore should be implemented by rather simple filter structures to optimize costs and power consumption. Simple hardware structures can be obtained by using cascaded integrator-comb (CIC) filters, which can be implemented using only registers and adders. The potential drawback of these filter type, the severe pass-band droop, can be compensated by using a simple equalizer filter at the end of the filter chain. The stop-band attenuation of the decimation filters are designed to fulfil the attenuation requirements of a 3^{rd}-order $\Delta\Sigma$-modulator, which requires a classical 4^{th}-order CIC filter in the first stage.

For the lower decimation stages filters with a steeper transition band are required. Hardware efficient realizations can be obtained by using half-band filters, with a symmetrical filter characteristic with respect to $f_s/4$ (f_s: sampling frequency). In this case 50% of the filter coefficients are zero and must not be realized. Furthermore, when properly designed, these filters can be clocked with the decimated sampling frequency. Since this filter stage is implemented as an ASIC or FPGA, MAC-operations should be avoided again. Very simple filter coefficients can be obtained by realizing the half-band filters by bireciprocal wave digital filters [7, 8, 10]. The transfer function of bireciprocal lattice wave digital filters, which are a special case of lattice WDFs, is given by:

$$H(z) = \left[H_0\left(z^2\right) + z^{-1} H_1\left(z^2\right)\right]/2. \qquad (12)$$

This filter type can be exploited to obtain efficient decimators for sampling rate conversion by two. The number of filter coefficients that must be implemented, is reduced by 50% and the filter can be clocked with the lower sampling frequency.

Similarly for the transfer function of N cascaded low order bireciprocal lattice wave digital filters following relationship holds, with all-pass filters $H_{i0}(z)$ and $H_{i1}(z)$:

$$H(z) = 2^{-N} \prod_{i=i}^{N} \left[H_{i0}\left(z^2\right) + z^{-1} H_{i1}\left(z^2\right)\right], \qquad (13)$$

where $H_{i0}(z)$ and $H_{i1}(z)$ are all-pass filters. Using this cascade connection of low order wave digital filter sections a number of advantages are obtained, compared to existing solutions.

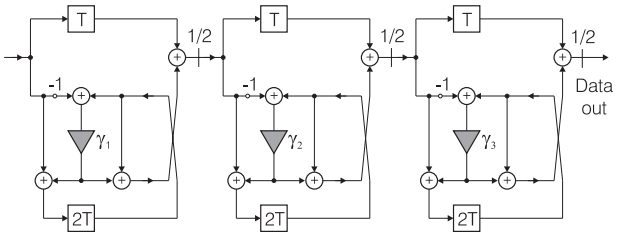

Fig. 8. Decimation stage consisting of 3 cascaded 3^{rd}-order bireciprocal wave digital filters.

Bireciprocal WDFs are minimum phase filters. They introduce however group delay distortion. By replacing one of the all-pass sections by a pure delay, a lattice WDF with approximately linear phase in the pass-band can be better approximated [16]. This holds since in the pass-band of the filter the responses of the all-pass sub-filters must be approximately equal. Since one of the branches is a pure delay, the phase response of the overall filter has approximately a linear phase in the pass-band. This will be taken into account by cascading 3^{rd}-order cells of bireciprocal lattice wave digital filters, as shown in Fig. 8, resulting in a superior group delay performance compared to a direct realization of a lattice WDF.

Cascading low-order sections, a high stop-band attenuation can be obtained with low coefficient sensitivity. Thus the optimized coefficients can be represented by very simple values and a wordlength of only a few bits is required. Due to the very simple coefficient representation no general multiplier is needed, thus minimizing the implementation costs. Furthermore the shorter wordlength also holds for the signal representation, resulting in reduced implementation costs for the adders and registers [9]. Since the cascaded low-order sections are very modular they are very attractive for VLSI-implementation.

The decimation stages had been designed for a minimum stop-band attenuation of about 95 dB, to account also for higher dynamic range requirements, which can be fulfilled by a higher sampling frequency of the modulator. The strongest requirements hold for the last filter stage, which can be however clocked with the lowest clock-frequency. This 4^{th} filter stage had been designed for a normalised stop-band edge frequency of $f_c/f_s = 0.355$. For the 3^{rd} decimation stage this requirement could be slightly relaxed. The discrete coefficient optimization procedure however came up with the same filter as for the 4^{th} stage. The architecture of the digital filter for the 3^{rd} and 4^{th} decimation stages (see Fig. 8) consists of a cascade of three 3^{rd}-order bireciprocal WDF blocks, resulting in a total filter order of 9. The decimation by two is performed in the 3^{rd} block which can thus be clocked with the reduced sampling rate.

The 2^{nd} decimation stage has been designed for a minimum stop-band attenuation of 80 dB from 0.4 to 0.45 and of 95 dB from 0.45 to 0.5. The filter can be also implemented by the structure in Fig. 8, where only two cascaded 3^{rd}-order cells are needed, which results in an overall filter order of 6. The optimized values for the three lower decimation stages are listed in Table 6.

Table 6. Optimized finite-precision adaptor coefficients for the cascaded lattice WDFs.

$Coeff.$	$Stage2$	$Stage3$	$Stage4$
γ_1	$2^{-1}-2^{-3}$	$2^{-1}-2^{-4}$	$2^{-1}-2^{-4}$
γ_2	$2^{-1}-2^{-3}-2^{-5}$	$2^{-1}-2^{-4}$	$2^{-1}-2^{-4}$
γ_3	–	$2^{-1}-2^{-3}$	$2^{-1}-2^{-3}$

Besides one coefficient in stage 2, which needs two shift-and-adds, all coefficients can be represented by only one shift-and-add operation. Since the decimation by 2 is implemented with the last filter cell of each decimation stage, stage 2 can be realized by 4 registers and 11 shift and operations. A wordlength of only 6 bits is required for the coefficient representation. For the realization of the 3^{rd} and 4^{th} stage 7 registers, 12 adders and 3 shift and add operations are needed for each stage. For the respective coefficients a wordlength of only 5 bits is required.

The attenuation requirements of the 4^{th} decimation stage can be also fulfilled by a classical 9^{th}-order bireciprocal WDF, which requires however 4 registers, 13 adders and 12 shift and add operations. Especially the wordlength of 12 bits necessary for the coefficient representation results in increased hardware costs. Furthermore the attenuation requirements can be fulfilled by an FIR-half-band filter of order 27, with 15 coefficients unequal to zero. For the coefficient representation a wordlegth of about 20 bits is necessary. Thus this filter type results in even more hardware costs and additional group delay. The results show, that compared to classical solutions, a considerable hardware reduction has been obtained using the cascaded low order sections.

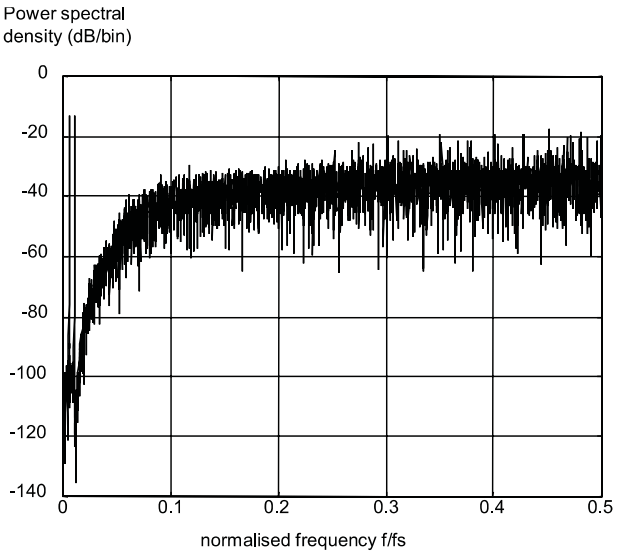

Fig. 9. Spectrum at modulator output using a sinusoidal IF-signal as input.

7. Performance results

Figure 9 shows the output spectrum of the modulator for a sinusoidal input signal shifted to an IF-frequency in the middle of the pass-band. A maximum SNR-value of 76 dB is obtained for the optimized A/D-converter with an over-sampling ratio of 32, where an additional improvement of 3 dB is obtained in the receiver due to the quadrature signal processing using two A/D-converters. The overload point is given by $O_L = 0.55$, thus the maximum amplitude of the input signals must be limited to this value.

To analyze the behavior of the modulator in the presence of out of band signals in adjacent channels, two GMSK-modulated signals in the first and second adjacent channels had been used as inputs. The respective modulator output spectrum is shown in Fig. 10. The results confirm, that neither the in-band noise nor the out-of-band noise at the modulator output are considerably increased using broadband input signals, which are typical for the digital receiver concept considered.

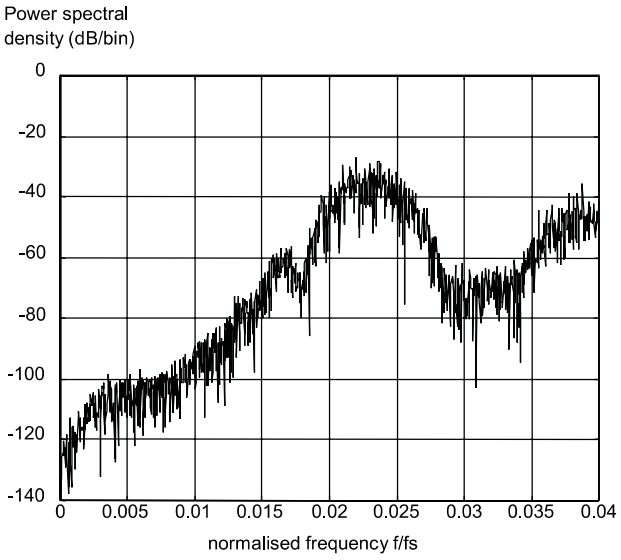

Fig. 10. Spectrum at modulator output with two GMSK-modulated adjacent channel signals.

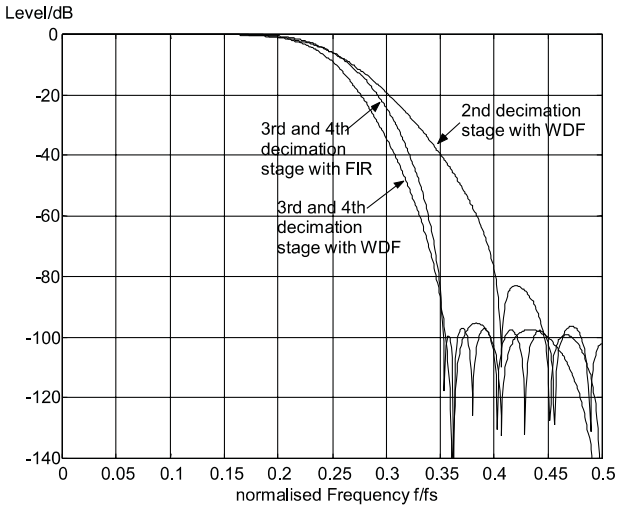

Fig. 11. Frequency response of the lower decimation stages.

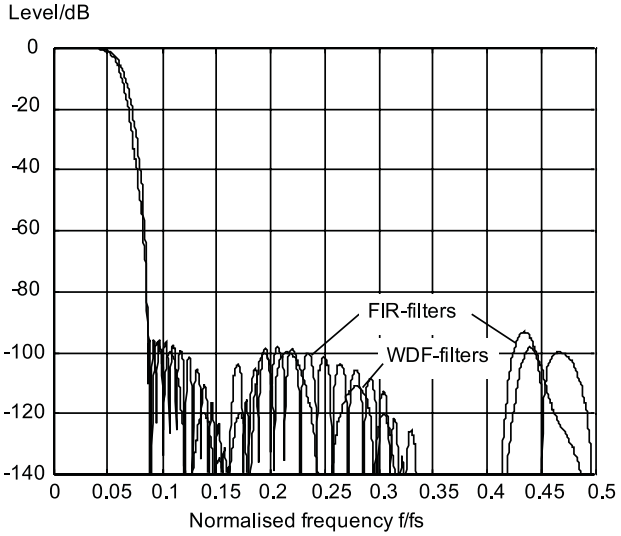

Fig. 12. Overall frequency response of the three lower decimation stages, curve (1): low order WDFs, curve (2): FIR-half-band filters.

Figure 11 shows the frequency responses of the lower decimation stages. The 2^{nd} filter stage is realized by two cascaded bireciprocal lattice WDFs of order 3 each. The 3^{rd} and 4^{th} filter stages consist of 3 cascaded 3^{rd}-order WDFs. For comparison purposes the transfer characteristic of a 27^{th}-order FIR-half-band filter is also shown in Fig. 11. It fulfils the requirements of the 3^{rd} and 4^{th} filter stages too.

Figure 12 shows the overall frequency response of the three lower decimation stages. A minimum attenuation of 96 dB is obtained. When cascaded with the first decimation stage, the minimum attenuation is even higher.

8. Summary

The design and optimization of the components for a flexible digital receiver for use in wireless communications systems has been presented. The optimization process includes the modulator of the $\Delta\Sigma$-A/D-converter and the decimation filter stages. It has been shown that very efficient realizations for the lower decimation stages can be obtained, by using cascaded low-order wave digital filters. The components have been optimized for a cost effective, combined FPGA/ASIC and processor implementation with the flexibility required by the application. The receiver concept is based on a low-IF architecture with channel filtering in the digital domain to allow flexibility and a complete integration of RF and baseband functionalities into a single integrated circuit in CMOS.

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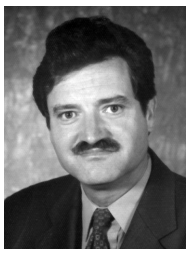

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