Optimised Decimation Stages with Lattice Wave Digital Filters for a Flexible Digital Receiver Architecture

Dieter Brückmann
Department of Electrical Engineering and Information Technology
University of Wuppertal, D-42097 Wuppertal, Rainer-Gruenterstr. 21, Germany
email: brueckm@uni-wuppertal.de

Abstract

In a digital receiver with broadband signal sampling digital decimation filters are required. The signal is sampled and digitised in such an architecture by a properly designed quantiser and the decimation stages behind the quantiser should be designed programmable to account for flexibility.
In this contribution a new architecture for the implementation of high-order, programmable decimation filters is described. Using this filter concept the flexibility with respect to multimode capability and the degree of integration can be drastically increased. It will be shown, that the use of cascaded low-order wave digital lattice filters for the lower decimation filter stages results in a number of advantages compared to standard methods. By properly selecting the number of lattice filter cells and optimising the filter coefficients, a very efficient realization is possible in VLSI-technology. Due to the simple filter structures and since no general multiplier is needed, significant hardware reduction can be obtained compared to existing solutions.

1. Introduction

In the field of mobile communications a number of new services and applications will come up in the next years, which will be covered by a variety of existing or new standards. These standards can have very different requirements with respect to bandwidth, dynamic range and so forth. To account for the future requirements flexible but low cost terminals with low power consumption and small size will be needed.

Multi-standard capability can be achieved by performing channel selection in the digital domain, where it can be implemented by programmable digital filters. The A/D-converter in such a concept digitises the wideband input signal containing the desired channel together with the unwanted adjacent channel interferers.

It has been shown, that very effective solutions are obtained when using ΔΣ–modulators with oversampling for the digitization. In such a concept no additional filtering for channel selection is required since the adjacent channel interferers are suppressed by the decimation stages together with the high-pass shaped quantisation noise. A further advantage results from the reduced requirements to the anti-aliasing low-pass filter due to oversampling.

To obtain optimum performance for the receiver together with minimum hardware effort the decimation stages must fulfil some requirements, which should be taken into account during the filter design process.

The decimation filters should be optimised for a FPGA- or ASIC-implementation [1, 2] to account for the very stringent cost and low power requirements in a mobile terminal. This means multiplications and MAC-operations, available in a general purpose DSP, should be avoided.

Furthermore the decimation ratio of the filters should be adjustable so that the required flexibility with respect to the bandwidth and/or dynamic range is obtained.

The group delay of the filters should be minimum in order to allow the implementation of a fast AGC in the receiver.

Finally no significant group delay distortion may be introduced in the passband.

Various filter structured had been proposed for the decimation stages of ΔΣ-modulators [3, 4]. All these solutions however do not fulfil the above mentioned requirements completely. Therefore in this contribution novel decimation filters will be proposed, which better fit the above requirements. It will be shown that properly designed cascade connections of low order lattice wave digital filters are especially well-suited for the lower decimation stages.

Lattice wave digital filters consist of a parallel connection of allpass sections [5, 6]. They have several advantageous properties, such as low coefficient sensitivity in the passband, low roundoff noise and the absence of parasitic oscillations. Furthermore they are minimum phase recursive filters.

A disadvantage however can be the high sensitivity in the stopband with respect to the coefficient truncation. For a high stopband attenuation many bits are required for the coefficient representation. This problem can be avoided by using cascade connections of low order wave digital subfilters [7], as will be shown in this contribution.

0-7803-6490-2/01/$10.00 ©2001 IEEE

Furthermore it will be shown that group delay distortion in the passband typical for recursive filters, can be reduced, by implementing one of the allpass sections by a pure delay.

2. Digital filter stages in a flexible receiver

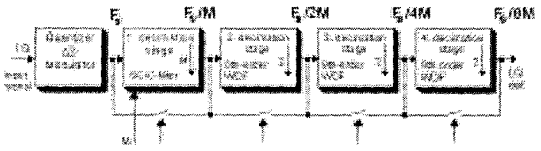

Figure 1: Receive path with decimation filters.

Fig. 1 shows the architecture of the digital part of the receive path considered [9]. Quadrature down conversion to baseband is performed in the analogue domain. The channel of interest is thus centred around DC. The I and Q components of the broadband receive signal are digitised by ΔΣ-modulators and channel-selection is then performed by the decimation filters, together with the suppression of the highpass-shaped quantisation noise.

It is well-known that the hardware required for the decimation filters can be minimised by performing decimation in several stages, with sample rate reduction after each stage. The first filter stage performs decimation by a programmable factor M. The following 3 stages each reduce the sampling rate by a factor of 2.

As shown in fig. 1, the decimation ratio is programmable in a wide range since each decimation stage can be also bypassed, and the decimation factor M of the upper stage is adjustable. Since the decimation stages are designed such that the lowest stage fulfils the most stringent attenuation requirements, bypassing of one or two lower stages should be performed such that stage 4 is bypassed at first and then the preceding stages.

The uppermost decimation stage is running at the highest clock frequency and therefore should be implemented by rather simple filter structures for minimum costs and power consumption. Simple hardware structures can be obtained by using cascaded integrator-comb (CIC) filters which can be implemented by using only registers and adders. The potential drawback of these filter type, the severe passband droop, which is dependant on the decimation ratio, can e.g. be avoided by using the so-called sharpened CIC-filter (SCIC) [9,10]. It requires only slightly more hardware, but shows considerably improved performance in the passband.

The stopband attenuation of the decimation filters are designed to fulfil the attenuation requirements of a 4th-order ΔΣ-modulator, which requires in the first stage a classical 5th-order CIC filter or a respective SCIC-filter.

For the lower decimation stages filters with a steeper transition band are needed. Very hardware efficient realizations are obtained by using optimised bireciprcal wave digital filters, as described in the next chapter.

3. Decimation filters composed of cascaded low order lattice wave digital filters

The lower decimation stages can be very efficiently implemented by cascaded low-order bireciprocal lattice wave digital filters. Bireciprocal lattice wave digital filters are a special case of lattice WDFs and have a symmetrical filter characteristic with respect to $F_s/4$ (F_s: sampling frequency). The transfer function of these filters is given by

$$H(z) = \frac{H_0(z^2) + z^{-1}H_1(z^2)}{2} \qquad (3.1)$$

which can be exploited to obtain efficient decimators for sampling rate conversion by two. The number of filter coefficients, that must be implemented, is reduced by 50% and the filter can be clocked with the lower sampling frequency.

Similarly for the transfer function of N cascaded low order bireciprocal lattice wave digital filters following relationship holds, with allpass filters $H_{i0}(z)$ and $H_{i1}(z)$.

$$H(z) = 2^{-N}\prod_{i=i}^{N}[H_{i0}(z^2) + z^{-1}H_{i1}(z^2)] \qquad (3.2)$$

where $H_{i0}(z)$ and $H_{i1}(z)$ are allpass filters.

Using this cascade connection of low order wave digital filter sections a number of advantages are obtained, compared to existing solutions.

Bireciprocal WDFs are minimum phase filters. They introduce however group delay distortion. By replacing one of the allpass sections by a pure delay a lattice WDF with approximately linear phase in the passband can be better approximated [11]. This holds since in the passband of the filter the responses of the all-pass subfilters must be approximately equal. Since one of the branches is a pure delay, the phase response of the overall filter has approximately a linear phase in the passband. This will be taken into account by cascading 3rd-order cells of bireciprocal lattice wave digital filters, as shown in fig. 2, resulting in a superior group delay performance compared to a direct realization of a lattice WDF.

Cascading low-order sections a high stopband attenuation can be obtained with low coefficient sensitivity. Thus the optimized coefficients can be represented by very simple values and a wordlength of only a few bits is required. Due to the very simple coefficient representation, no general multiplier is needed, thus minimizing the implementation costs. Furthermore the shorter wordlength also holds for the signal representation, resulting in reduced implementation costs for the adders and registers [7].

Furthermore the cascaded low-order sections are very modular, making it very attractive for VLSI-implementation.

The decimation stages had been designed for a minimum stopband attenuation of about 95dB. The strongest requirements hold for the last stage, which can be however clocked with the lowest clockfrequency. This 4th filter stage had been designed for a normalised stopband edge frequency of f_c/f_s=0.355. For the 3rd decimation stage this requirement could be slightly relaxed, the discrete coefficient optimization however came up with the same filter as for the 4th stage.

The architecture of the lattice wave digital filter for the 3rd and 4th decimation stages is shown in Fig. 2. It consists of a cascade of three 3rd-order bireciprocal WDF filter blocks, resulting in a total filter order of 9. The decimation by two is performed in the 3rd block which can thus be clocked with the reduced sampling rate.

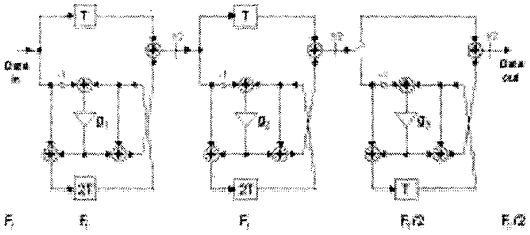

Figure 2: Decimation stage consisting of 3 cascaded 3rd-order bireciprocal WDF-filters.

The 2nd decimation stage has been designed for a minimum stopband attenuation of 80dB from 0.4 to 0.45 and of 95dB from 0.45 to 0.5. The filter can be also implemented by the structure in fig. 2, where only two cascaded 3rd-order cells are needed, which results in an overall filter order of 6.

The optimised values for the three lower decimation stages are listed in table 1. Besides one coefficient in stage 2, which needs two shift-and-adds, all coefficients can be represented by only one shift-and-add operation. Since the decimation by 2 is implemented with the last filter cell of each decimation stage, stage 2 can be realized by 4 registers and 11 shift and operations. A wordlength of only 6 bits is required for the coefficient representation.

Table I
OPTIMIZED FINITE-PRECISION ADAPTOR COEFFICIENTS FOR THE CASCADED LATTICE WDFs

Stage 2	Stage 3	Stage 4
$g_1 = 2^{-1} - 2^{-3}$	$g_1 = 2^{-1} - 2^{-4}$	$g_1 = 2^{-1} - 2^{-4}$
$g_2 = 2^{-1} - 2^{-3} - 2^{-5}$	$g_2 = 2^{-1} - 2^{-4}$	$g_2 = 2^{-1} - 2^{-4}$
----	$g_3 = 2^{-1} - 2^{-4}$	$g_3 = 2^{-1} - 2^{-4}$

For the realization of the 3rd and 4th stage 7 registers, 12 adders and 3 shift and add operations are needed for each stage. For the respective coefficients a wordlength of only 5 bits is required.

The attenuation requirements of the 4th decimation stage is also fulfilled by a classical 9th-order bireciprocal WDF, which requires however 4 registers, 13 adders and 12 shift and add operations. Especially the necessary wordlength of 12 bits for the coefficient representation results in increased hardware costs.

Furthermore the attenuation requirements can be also fulfilled by an FIR-halfband filter of order 27, with 15 coefficients unequal to zero. For the coefficient reprensentation a wordlegth of about 20 bits is necessary. Thus this filter type results in more hardware costs and additional group delay. The results show that, compared to classical solutions, a considerable hardware reduction has been obtained using the cascaded low order sections.

4. Simulation results

Fig. 3 shows the frequency responses of the lower decimation stages. The 2nd filter stage is realized by two cascaded bireciprocal lattice WDFs of order 3 each. The 3rd and 4th filter stages consist of 3 cascaded 3rd-order WDFs. For comparison purposes the transfer characteristic of a 27th-order FIR-halfband filter is also shown in fig. 3. It fulfils the requirements of the 3rd and 4th filter stages too.

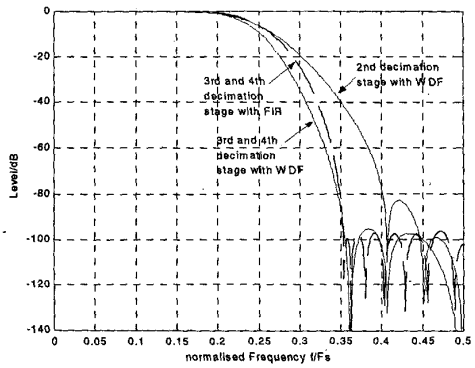

Figure 3: Frequency responses of the lower decimation stages

Fig. 4 shows the overall frequency response of the three lower decimation stages. A minimum attenuation of 96dB is obtained. When cascaded with the first decimation stage, the minimum attenuation is even higher.

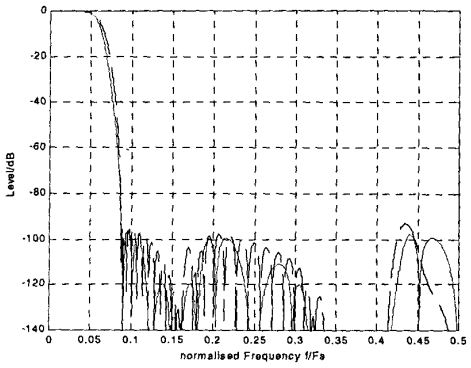

Figure 4: Overall frequency response of the three lower decimation stages,
solid line: cascaded low order WDFs,
dashed line: FIR-halfband filters.

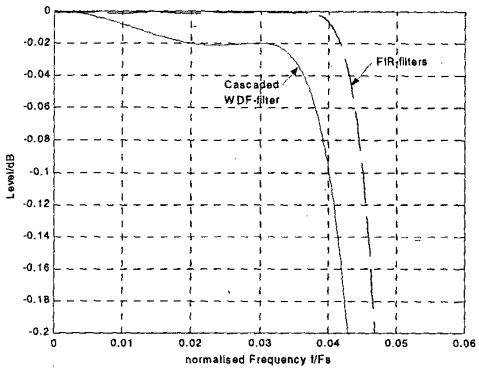

Figure 5. Passband behaviour of the three lower decimation stages,
solid line: cascaded low order WDFs,
dashed line: FIR-halfband filters..

The overall passband behaviour of the lower decimation filters is shown in fig. 5. Due to the excellent passband performance of bireciprocal WDFs, the ripple is smaller than 0.05dB which is more then sufficient for the application.

The resolution required for the ADCs of the digital receiver is determined by the dynamic range requirements of the receive path. If the RF-front end is designed properly, the required dynamic range can be obtained from the smallest wanted and the largest unwanted signal which must be processed in common. The respective values can be found in the physical layer specification of the various wireless and mobile standards as interferer and blocking requirements.

5. Conclusions

In this contribution a novel decimation filter architecture has been proposed for the realization of highly optimised but flexible digital receivers. It has been shown that very effective realizations for the lower decimation stages can be obtained, by using cascaded low-order wave digital filters. This filter type can be implemented with minimum hardware compared to other solutions such as classical wave digital filters or FIR-filters.

Further advantages of the proposed filter structures are superior sensitivity properties with respect to coefficient quantisation effects, better noise performance and less group delay distortion compared to classical structures.

References

[1] M. Cummings and S. Haruyama, "FPGA in the Software Radio," IEEE Communication Magazine, Feb. 1999, vol. 37, no. 2, pp. 108-112.

[2] C. Dick and F.J. Harris, "Configurable Logic for Digital Communications: Some Signal Processing Perspectives," IEEE Communication Magazine, Aug. 1999, vol. 37, no. 8, pp. 112-117.

[3] S. R. Northworthy, R. Schreier, G. C. Temes: "Delta-Sigma Data Converters, Theory Design and Simulation", IEEE Press, New York, 1997.

[4] I. Kale, R. C. S. Morling, A. Krukowski and C. W. Tsang, "A High-Fidelity Decimator Chip for the Measurement of Sigma-Delta Modulator Performance, IEEE Transactions on Instrumentation and Measurement, vol. 44, no. 5, pp. 933-939, Oct. 1995.

[5] A. Fettweis, "Wave Digital Filters: Theory and Practice", Proceedings of the IEEE, vol. 74, no. 2, pp. 270-327, Feb. 1986.

[6] L. Gazsi, "Explicit formulas for lattice wave digital filters", IEEE Trans. Circuits Syst., vol. CAS-32, no. 2, pp. 68-88, Jan. 1985.

[7] J. Y. Kaakinen and T. Saramäki, "Design of Very Low-Sensitivity and Low-Noise Recursive Filters Using a Cascade of Low-Order Lattice wave Digital Filters, IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing, vol. 46, no. 7, pp. 906-914, July 1999.

[8] D. Efstathiou, J. Fridman, and Z. Zvonar, "Recent Developments in Enabling Technologies for Software Defined Radio," IEEE Communication Magazine, Aug. 1999, vol. 37, no. 8, pp. 112-117.

[9] D. Brückmann, "Optimised Components for Flexible Digital Receivers with IF-Sampling", Proceedings 1st Karlsruher Workshop on Software Radios, pp. 1-6, Feb. 2000.

[10] A. Y. Kwentus, Z. Jiang, and A. N. Willson, "Application of Filter Sharpening to Cascaded Integrator-Comb Decimation Filters", IEEE Transactions on Signal Processing, vol. 45, no. 2, pp. 457-467, Feb. 1997.

[11] H. Johansson and L. Wanhammer, "Wave Digital Filter Structures for High-Speed Narrow-Band and Wide-Band Filtering, IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing, vol. 46, no. 6, pp. 726-741, June 1999.