DIGITAL FILTER DESIGN FOR A PAL TV MODULATOR

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ABSTRACT

This paper develops a multirate digital filter design for the Vestigial SideBand (VSB) modulator required in the analog TV transmission systems, like PAL. The design is based on a complex baseband VSB filter running at 13.5 MHz sampling rate, digital multirate techniques for increasing the sampling rate by the factor of 9, and a combination of multirate techniques and digital mixing to translate the signal to the 38.9 MHz IF picture carrier frequency.

1 INTRODUCTION

The traditional analog TV transmission systems have still a lifetime of many years, even though the new digital transmission techniques are being taken into use. In this situation, there is interest to more advanced implementation techniques for the traditional analog systems. For example, in CATV networks, the incoming TV signals are in many cases in digital format and also the modulators for new digital standards are using digital signal processing all the way to the IF stage.

In this paper we develop a PAL modulator based entirely on digital signal processing techniques. The proposed design is based on low-order recursive Nth-band filters [1]. First- and second-order allpass sections are used as basic building block for these filters. Therefore, the resulting structures are highly modular which makes them suitable for VLSI implementation. In addition, they are characterized by many attractive properties, such as a reasonably low coefficient sensitivity, a low roundoff noise level, and the absence of parasitic oscillations. Furthermore, these filters have turned out to be very efficient in sampling-rate conversion applications. It is also possible to design recursive Nth-band filters to have an approximately linear phase in the passband by selecting the one of the allpass subfilters to consist of pure delay elements [1].

In highly customized VLSI implementations, a general multiplier is very costly. Therefore, it is attractive to carry out the multiplication of a data sample by a filter coefficient using a sequence of hard-wired shifts and adds [2]. This leads to a significant reduction in computational complexity, power consumption, and silicon area. The resulting design is quite feasible for implementation as an ASIC or even on an FPGA circuit.

2 OVERALL STRUCTURE

The input signal is assumed to be a composite baseband video signal with 13.5 MHz sampling rate. Further, it is assumed that the input video signal is bandlimited from the high frequency end in such a way that there are no signal components which would disturb the audio carriers to be included in the complete TV signal. Therefore, there is no need to implement the upper stopband part of the specifications [3] here. This means also that the audio components could be included in the signal already before the VSB filter. A suitable digital implementation of an audio modulator is described in [4].

Figure 1 shows the overall block diagram of the proposed VSB modulator. The DC-level of the input signal can be used to control the residual carrier level. After the VSB filtering the signal consist of the in-phase (I) and quadrature (Q) components. The I/Q signal then passes through the interpolation and mixing section, which increases the sampling rate by the factor of 9 to 121.5 MHz using multirate filtering. In addition, the signal is simultaneously translated in the frequency domain to the usual 38.9 MHz picture carrier frequency. The frequency translation is done partly through the imaging effect of multirate signal processing, and partly through frequency translation by digital I/Q-mixing.

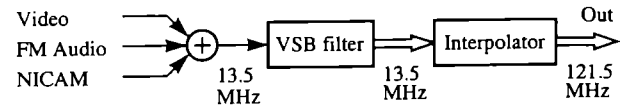

Fig. 1. Digital VSB modulator.

2.1. VSB Filter

The VSB filter is implemented as a complex baseband filter, which is quite feasible in case of digital signal processing. Figure 2 shows the structure of the multi-stage VSB filter, which is described in more details in [5]. The design is based on low-order approximately linear phase IIR Nth-band filter and Hilbert-transformer sections [1]. The required filter orders for the allpass sections are:

$H_1(z)$, $H_3(z)$: halfband filters, branch 1 is a 4th-order allpass; branch 2 is a pure delay

$H_2(z)$: 4th-band filter, branches 1, 2, and 3 are 2nd-order allpasses, branch 4 is a pure delay.

The filter coefficients have been optimized utilizing techniques described in [2]. Considering the sums of power-of-two coefficient representation, the number of additions needed to implement all the filter coefficients is 9. Notice that only the output of the filter is complex, all other parts are implemented using real signals.

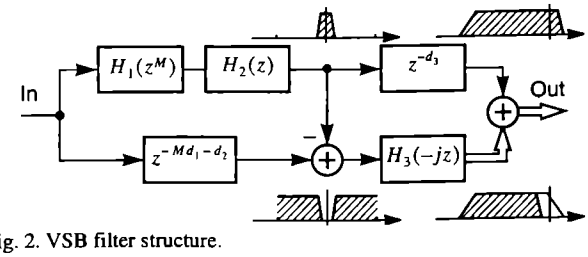

Fig. 2. VSB filter structure.

2.2. Interpolation and Mixing Algorithm

The interpolation and mixing process is illustrated in Fig. 4. By implementing the interpolation at two stages, the requirements for the anti-imaging filters can be reduced. The output of the VSB filter is transformed to a nearly symmetric baseband signal using digital I/Q-mixing. After the first interpolation by three, the undesired images are attenuated using 3rd-band filter $H_4(z)$. At the second stage, the signal is upconverted by multiplying it with $e^{j\pi k/4}$ and the sampling rate is further increased by 3. The resulting signal is filtered by $H_5(j\frac{2}{3}z)$ which is shifted version of the normal 3rd-band filter to attenuate undesirable images.

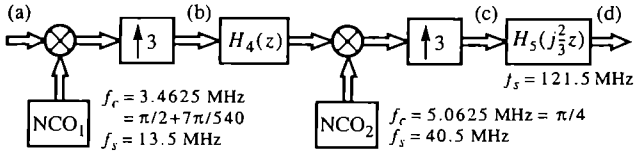

Fig. 3. Block diagram for the interpolation and mixing section.

2.3. Interpolation Filter Design

Approximately linear-phase IIR Nth-band filters are also used for interpolation filtering. In order to satisfy the adjacent channel rejection specifications, the stopband attenuation requirements for the 3rd-band filters are approximately 58 dB. The required orders for the allpass sections are: branches 1 and 2 are 4th-order allpasses; branch 3 is a pure delay. For $H_5(j\frac{2}{3}z)$, branches 1 and 2 are 2nd-order allpasses and branch 3 is a pure delay.

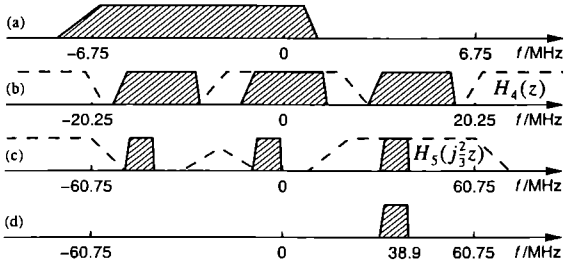

Fig. 4. Characteristic amplitude responses at the different stages of interpolation and mixing section.

Again the coefficients of the allpass subfilters were optimized such that the overall filter satisfies the given amplitude criteria with the simplest coefficient representation forms. Considering the sums of powers-of-two coefficient representation, a total of only 5 additions are required to implement all the filter multipliers for $H_4(z)$. In this case, 7 fractional bit are required to meet the specifications. The similar figures for $H_5(j\frac{2}{3}z)$ are 5 and 6. Figure 5 shows the magnitude response of the overall system as well as the magnitude response and group delay for the VSB filter.

The interpolation filtering may be implemented very efficiently using alternating switches, or commutative structures [1]. In this case, each of the subfilters is operating at the lower sample rate. This reduces the computational complexity per input sample remarkably.

2.4. Numerically Controlled Oscillator

The solution has been optimized in order to be able to use as simple NCO's (numerically controlled oscillators) as possible for generating the digital local oscillator signals. Since there is a rather simple fractional relation between the sampling rates and the NCO frequencies, the NCOs can be implemented by explicitly storing the needed sinusoidal signal sample values.

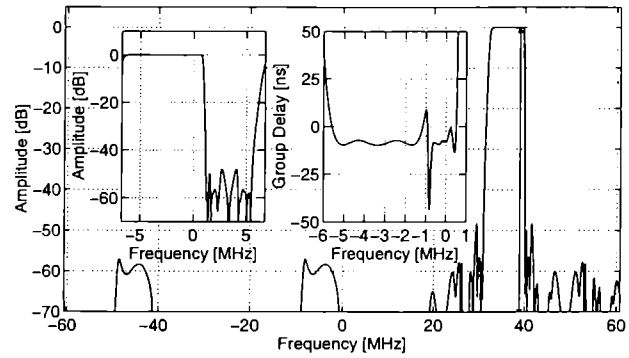

Fig. 5. Amplitude response for the overall design as well as the magnitude response and group delay for the VSB filter.

3 ASIC IMPLEMENTATION

After circuit design, a VHDL model for the VSB filter was constructed and simulated. The VHDL simulation results were compared with MATLAB simulation results to verify the performance of the designed circuits and to determine the additional bits needed to satisfy finite wordlength effects. In order to avoid overflows and to satisfy round-off noise requirements, three more additional bits are needed when input is 13 bits sinusoidal signal. Using 16 bit overall data wordlength (12 fractional bits, 3 integer bits and sign) in internal computations, the round-off noise level is well over 60 dB below the carrier power. A layout is currently under construction using standard-cell approach.

4 CONCLUSIONS

We have developed a VSB modulator design for the PAL specifications utilizing entirely digital signal processing. The design is based on low-order allpass filter sections and two simple NCO's and I/Q mixers. The design is quite feasible for implementation as an ASIC or even on an FPGA circuit.

ACKNOWLEDGEMENTS

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